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66	3V_AUX/5V_AUX/3V_PCIAUX
67	SFR / -12V
68	Vcore PWM
69	Vore driver
70	Vcore GT driver
71	VCCIO & VCCSA

Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

BOM DISTRIBUTION RULE
Frodo, SamWise
(BOM,BOM)

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DO NOT DISTRIBUTE

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

	Frodo	Samwise
PCH	Q87	Q85

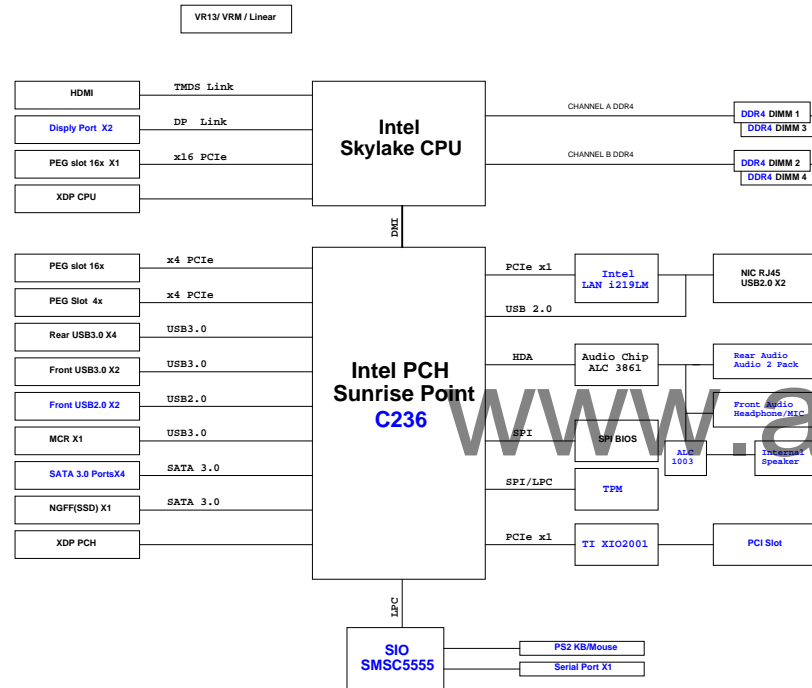
PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
EVT1	RED	YELLOW
EVT2	RED	WHITE
DVT1	LIGHT BLUE	YELLOW
DVT2+	LIGHT BLUE	WHITE
PVT1	GREEN	YELLOW
PVT2+	GREEN	WHITE
MVB / PRODUCTION	GREEN	WHITE

PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

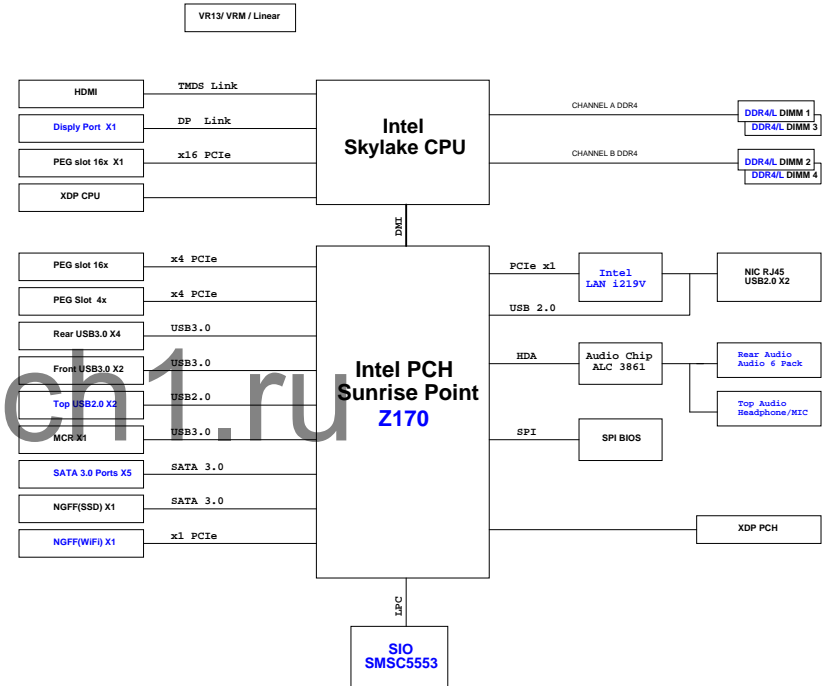


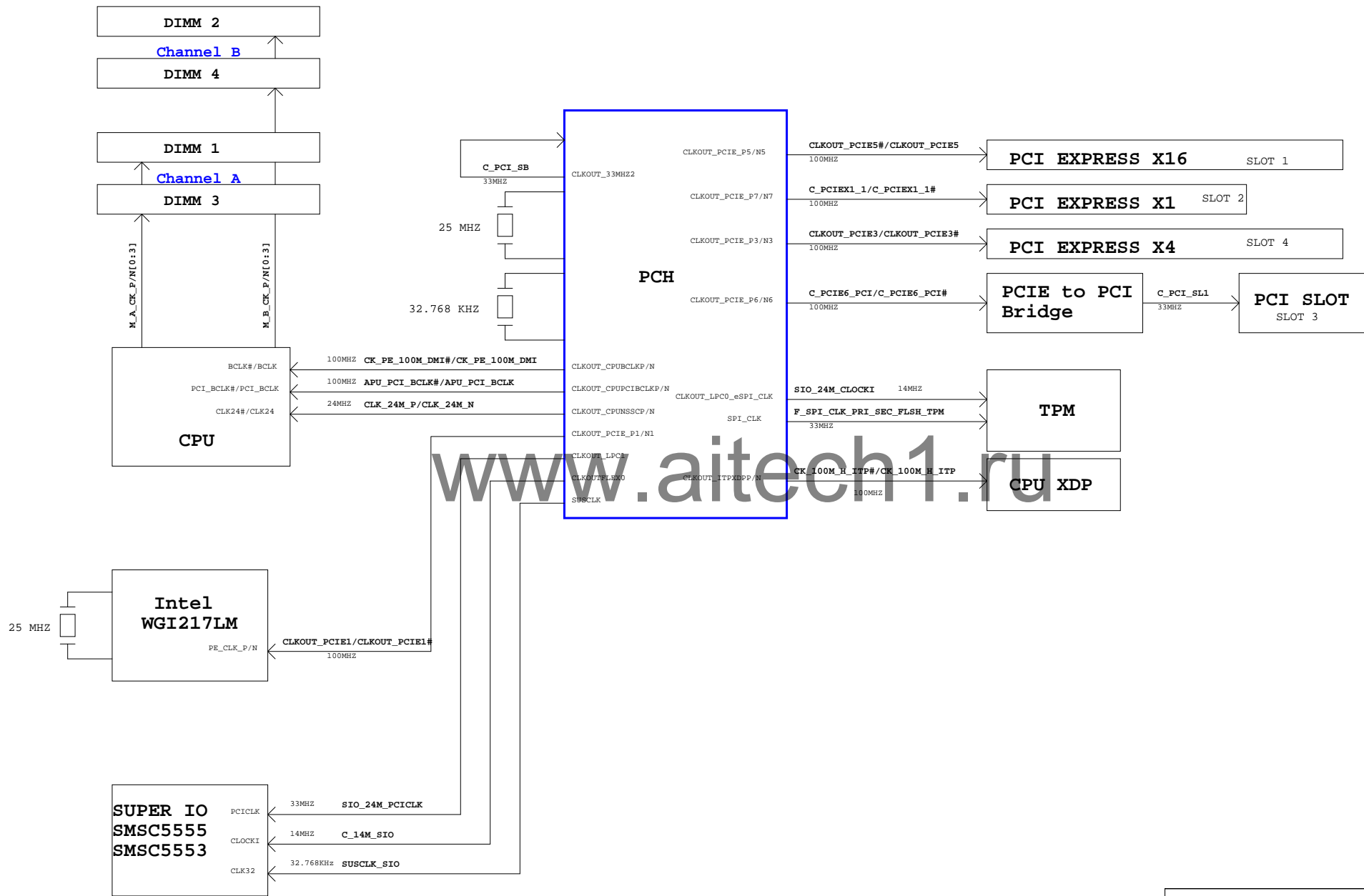
INDEX		
DWG NO	Rev	A00
GY SKL/ Farallon MT		
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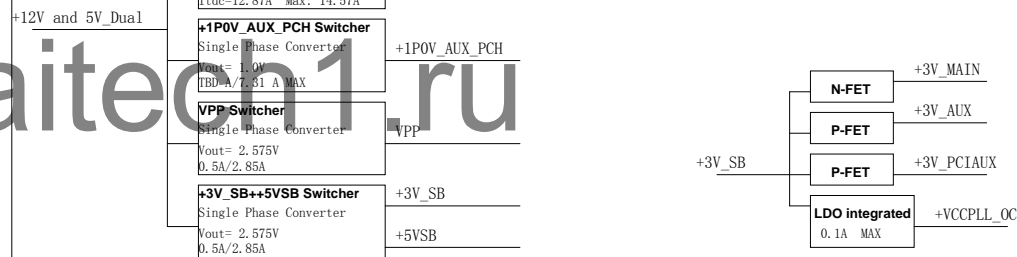
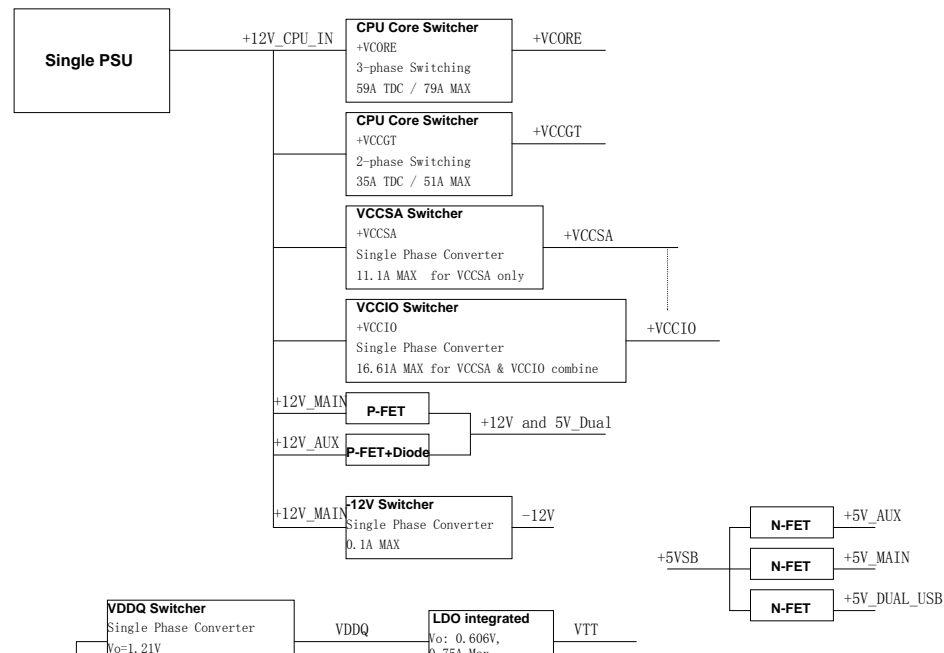
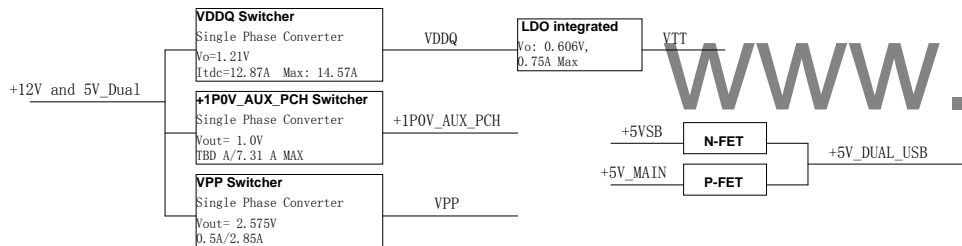
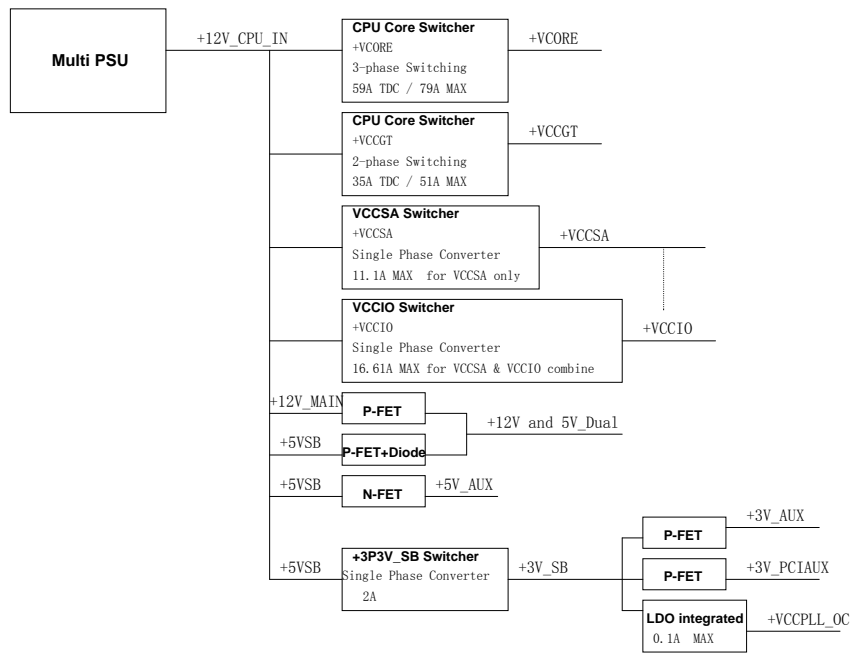
Farallon MT



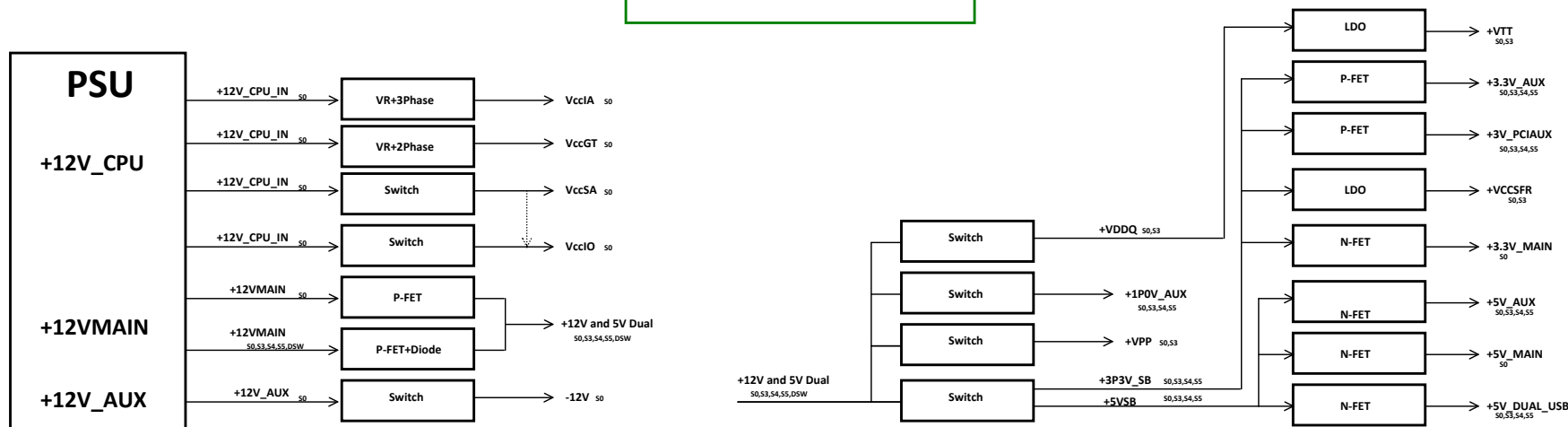
Goodyear SKL



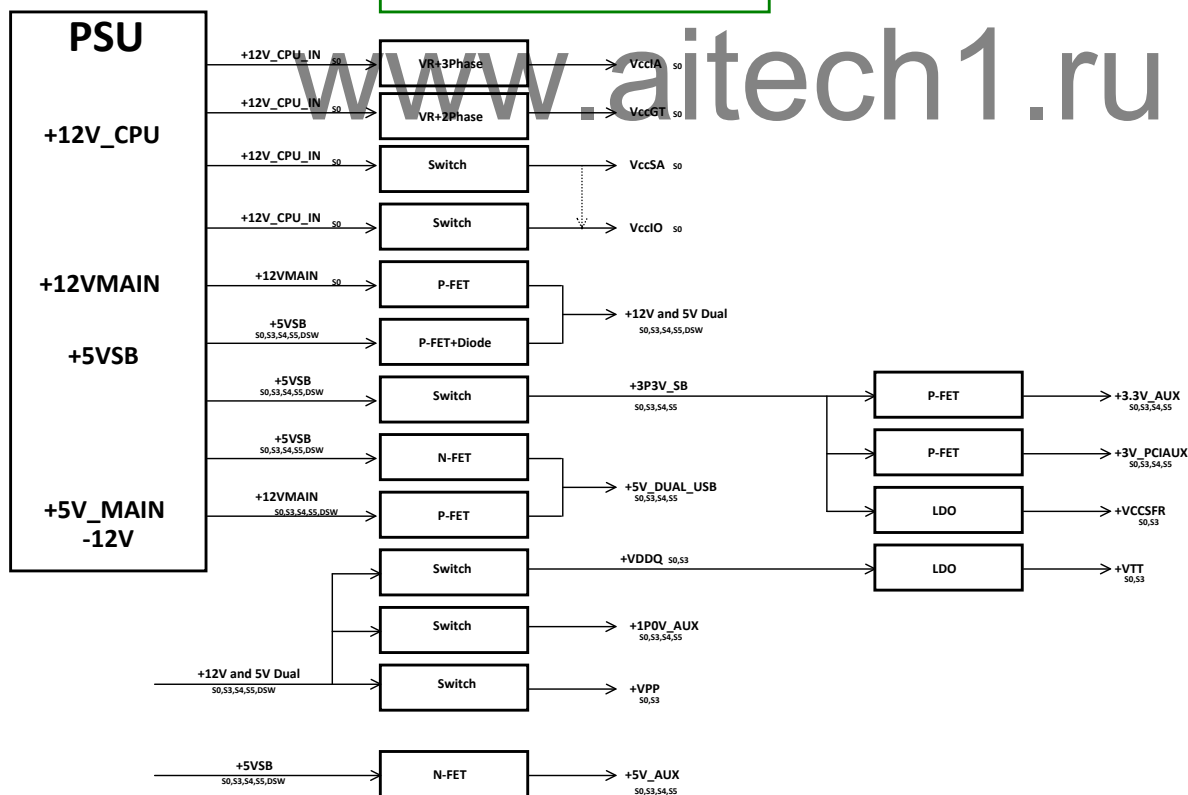




Farallon MT



Goodyear SKL



[illegible][illegible]

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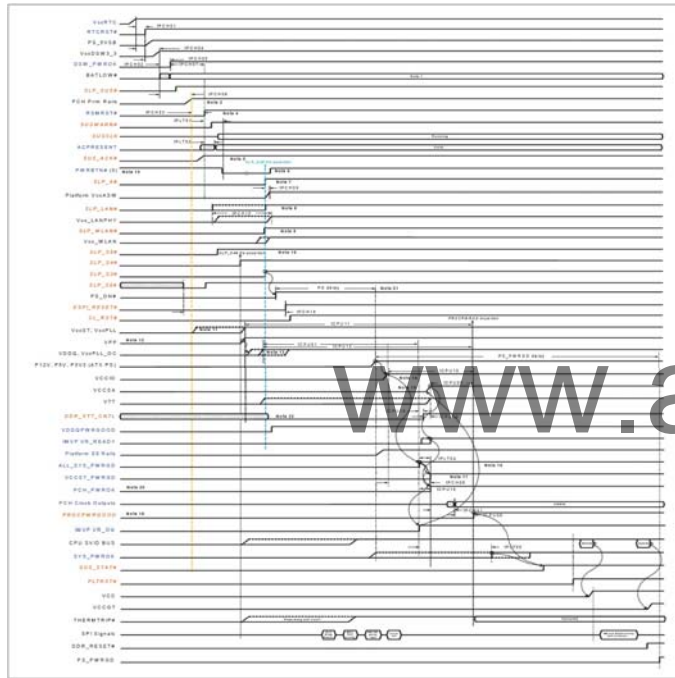
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0000_1700_0000 7 000_20	0000_1700_0000 7 000_20	0000_1700_0000 7 000_20	0000_1700_0000 7 000_20			
8		<table border="1"> <tr> <td>0000_1700_0000 8 000_20</td> <td>0000_1700_0000 8 000_20</td> <td>0000_1700_0000 8 000_20</td> <td>0000_1700_0000 8 000_20</td> </tr> </table>	0000_1700_0000 8 000_20	0000_1700_0000 8 000_20	0000_1700_0000 8 000_20	0000_1700_0000 8 000_20
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0000_1700_0000 10 000_20	0000_1700_0000 10 000_20	0000_1700_0000 10 000_20	0000_1700_0000 10 000_20			

[illegible]

POWER SEQUENCE DIAGRAM

SKL-S Timing Diagram for G3 to S0/M0 [Deep Sx Platform]

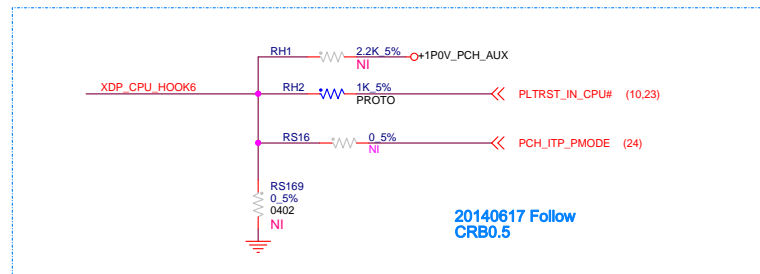
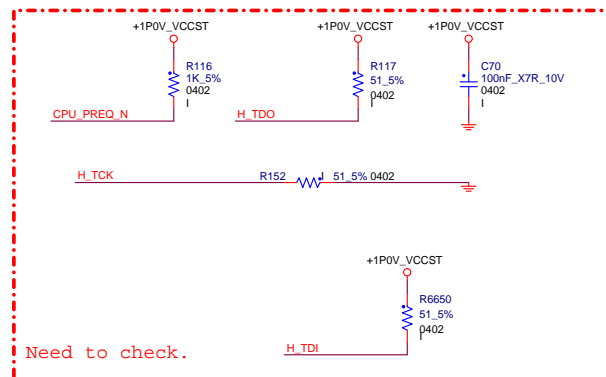


SKL-S Timing Diagram for S0/M0 to G3 [Deep Sx Platform]

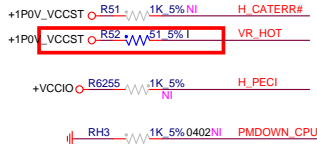
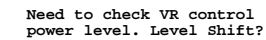


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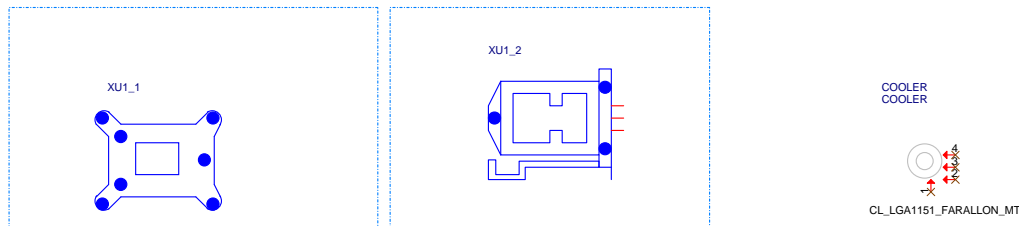
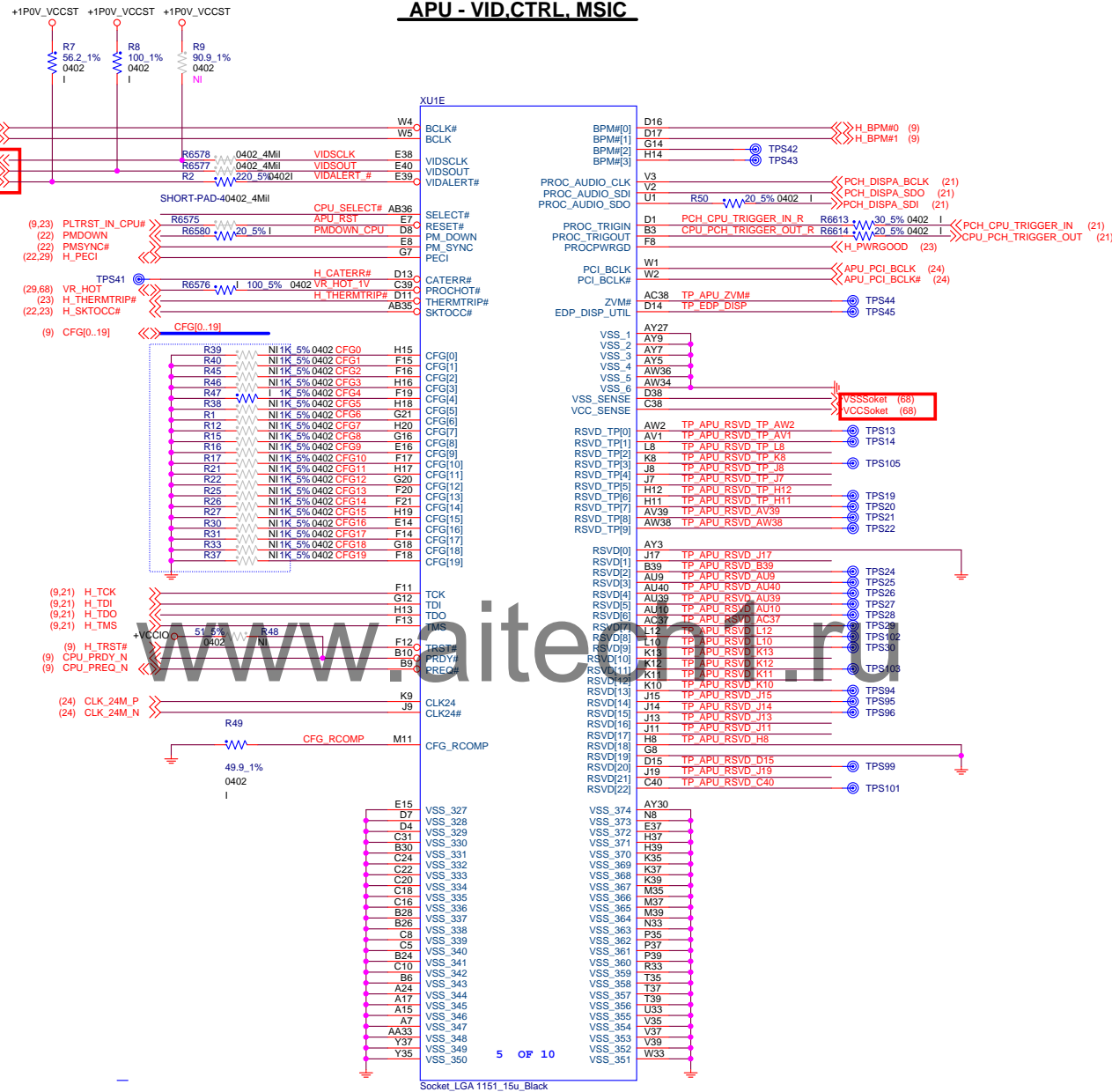
APU - VID,CTRL,MSIC



20140516 SKL-S EDS0.75:It should be connected to VCCIO with pull-up resistor of xx

PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG LANE REVERSAL
3	ENABLE	DISABLE	PHYSICAL DEBUG ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET N	BIOS REQ	PEG DEFER TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		
ALL PINS HAVE INTERNAL PULL-UPS			

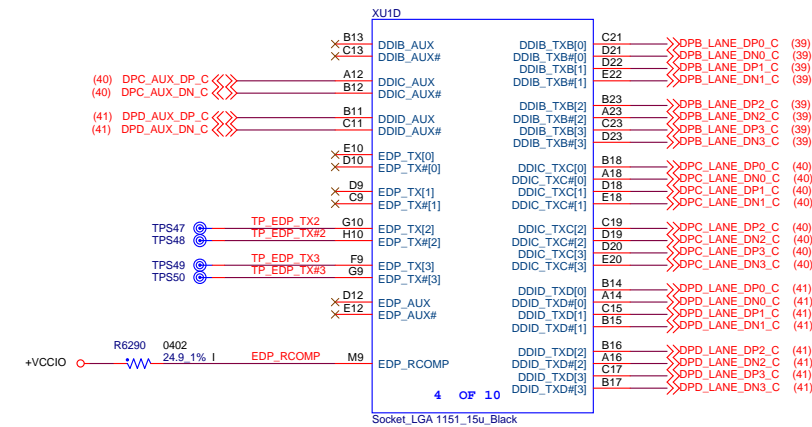
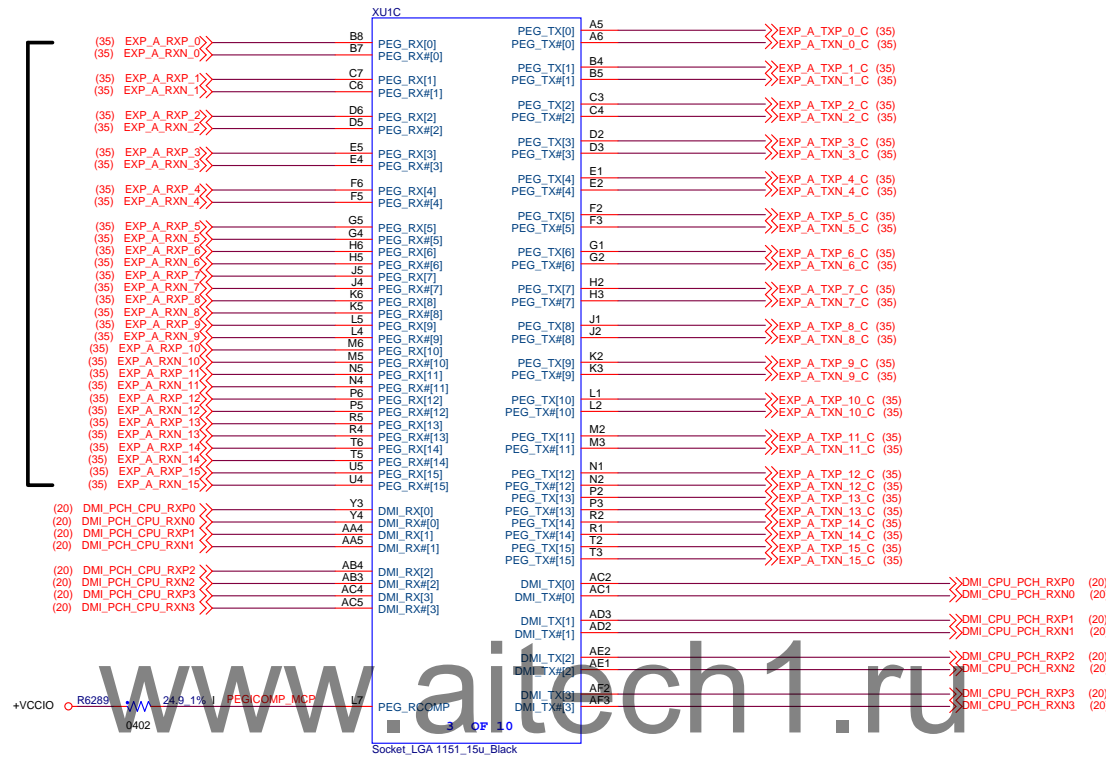


Title **CLK/ CTRL/ MISC/DEBUG**

DWG NO	Rev
<i>GY SKL/ Farallon MT</i>	A00

Date: Tuesday, July 07, 2015 Sheet 10 of 71

PEG AC Cap Value	
Gen1/Gen2	75nf~265nf
Gen3	180nf~265nf

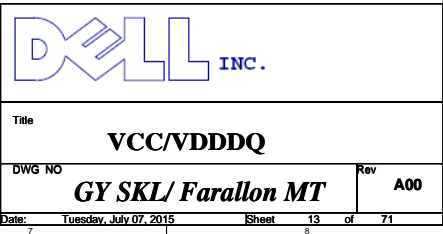


Processor PCI Express® Compensation Signal Routing Guidelines					
Parameter	Units	Trace width	Trace spacing to other signals	Routing Length	Resistance
PEG_RCOMP	mils	12	15	400	
Resistor	ohm				24.9+-1%



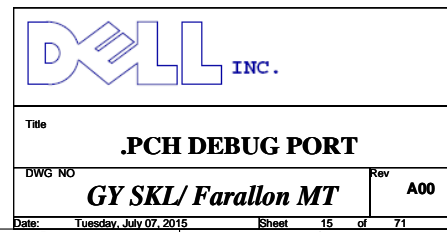
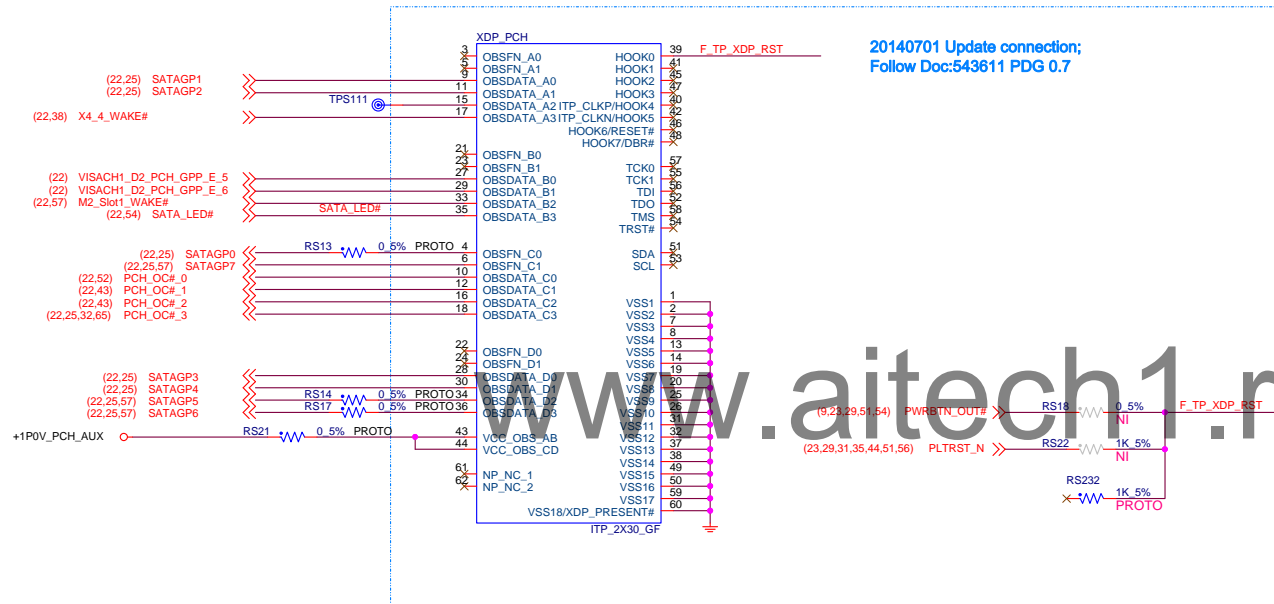
Title			
PCIE/ DMI/ DDI			
DWG NO	Rev		
GY SKL/ Farallon MT		A00	
Date:	Tuesday, July 07, 2015	Sheet	12 of 71

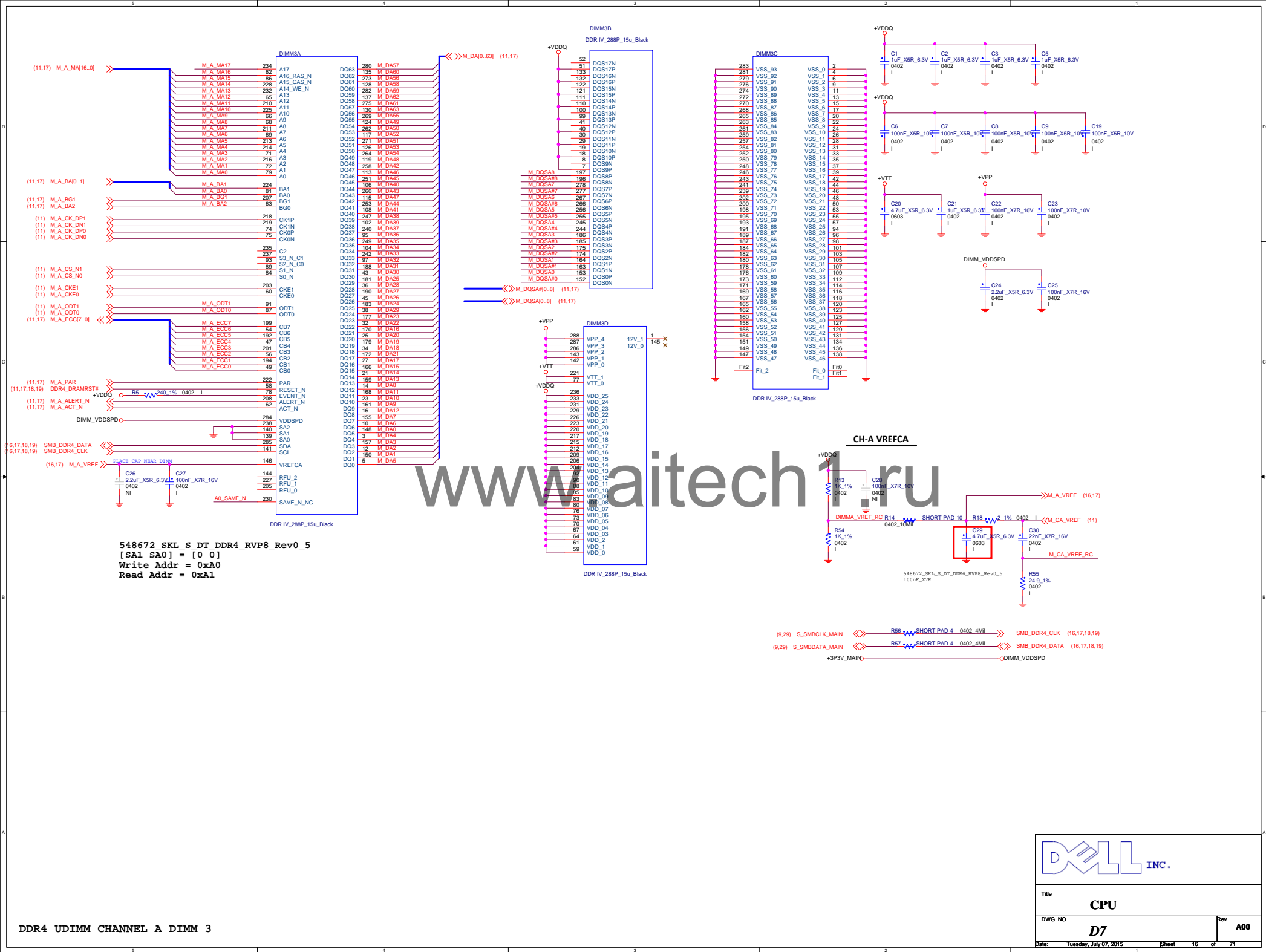
Foxconn Restricted Secret

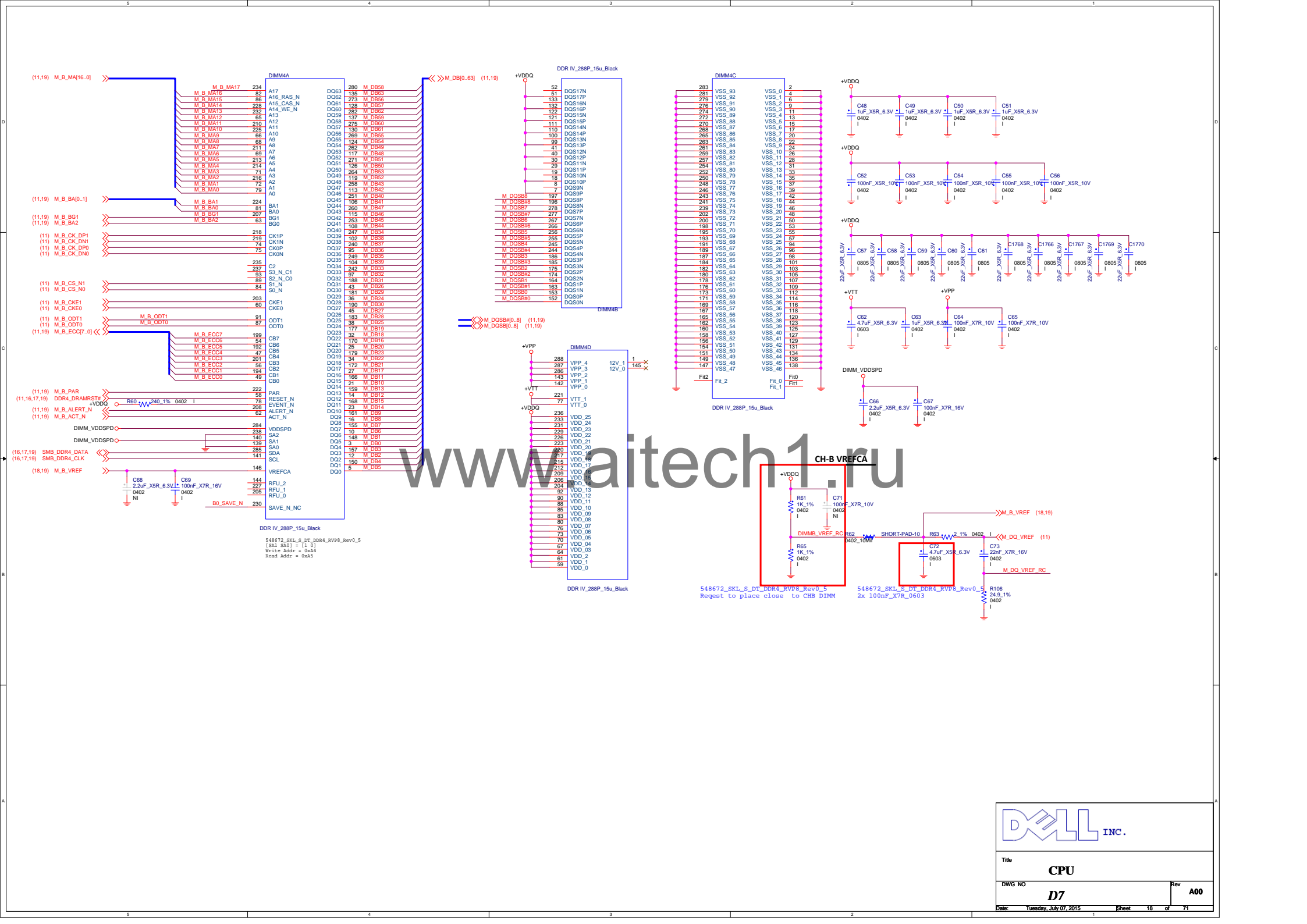




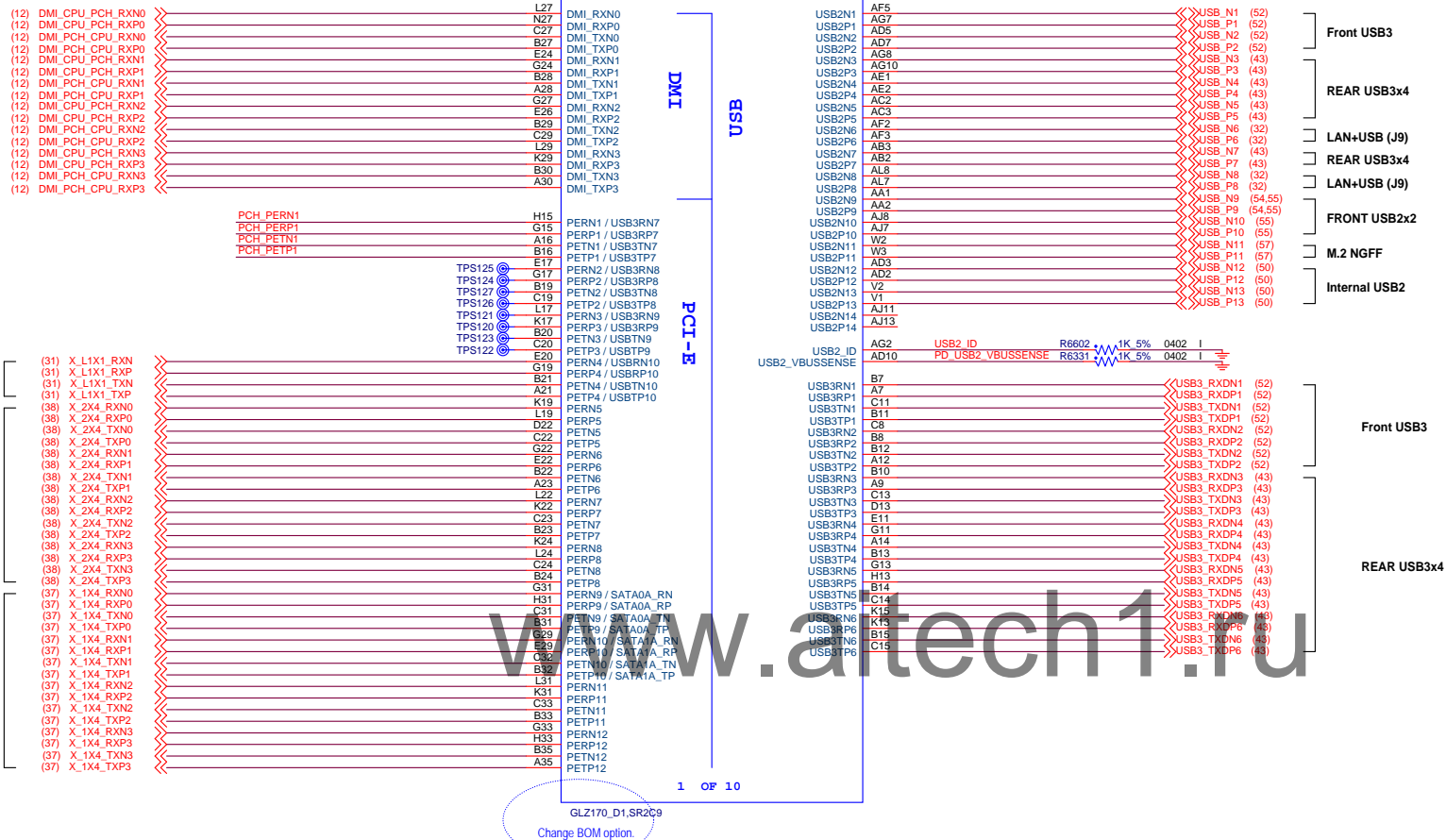
Intel PCH XDP Debug Connector



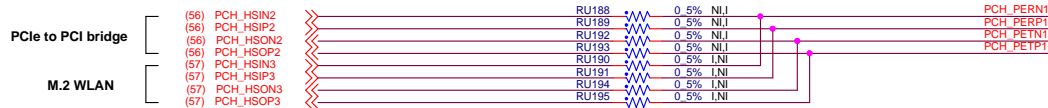




It is highly recommended to have DMI on surfaced vias (not buried).

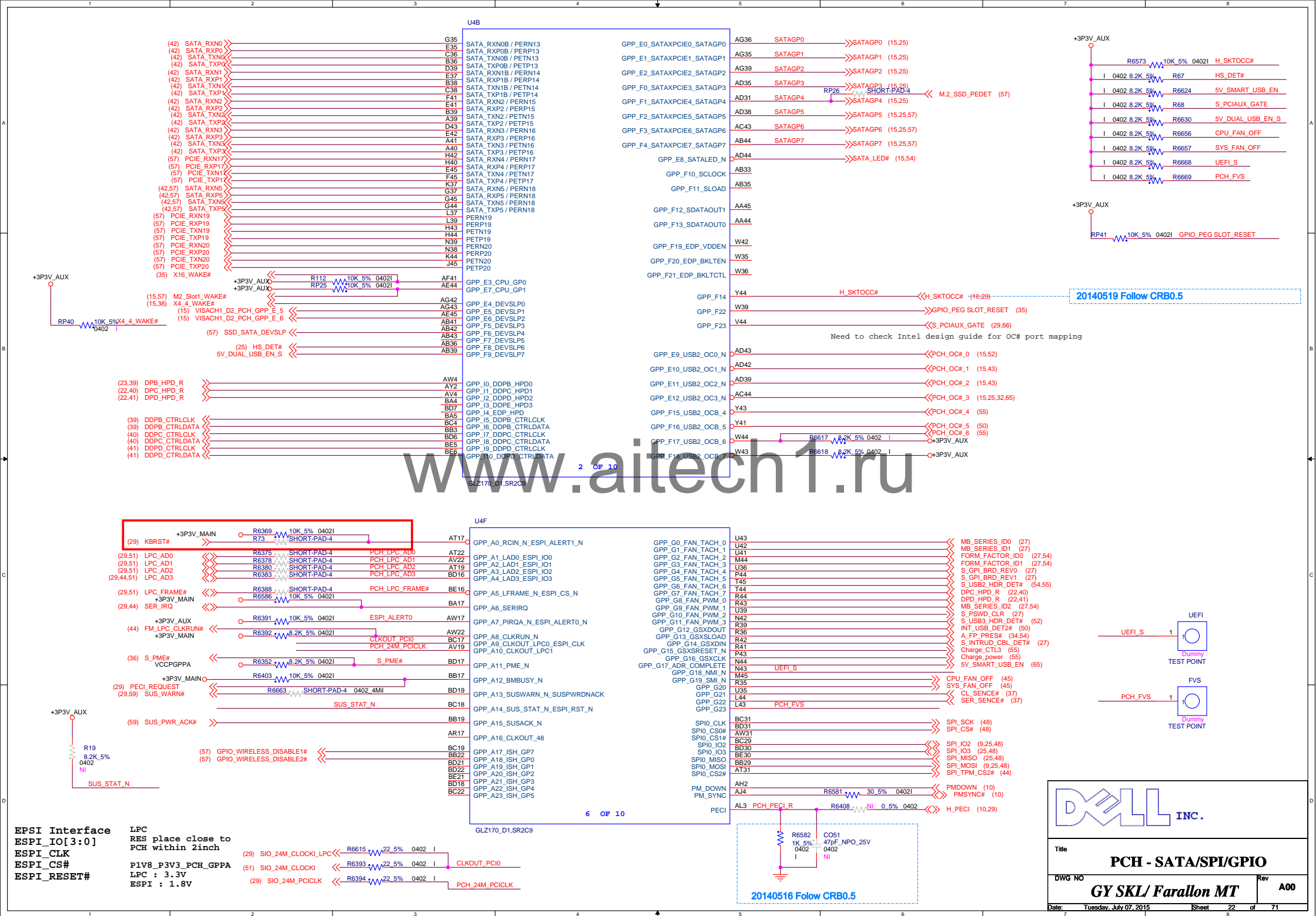


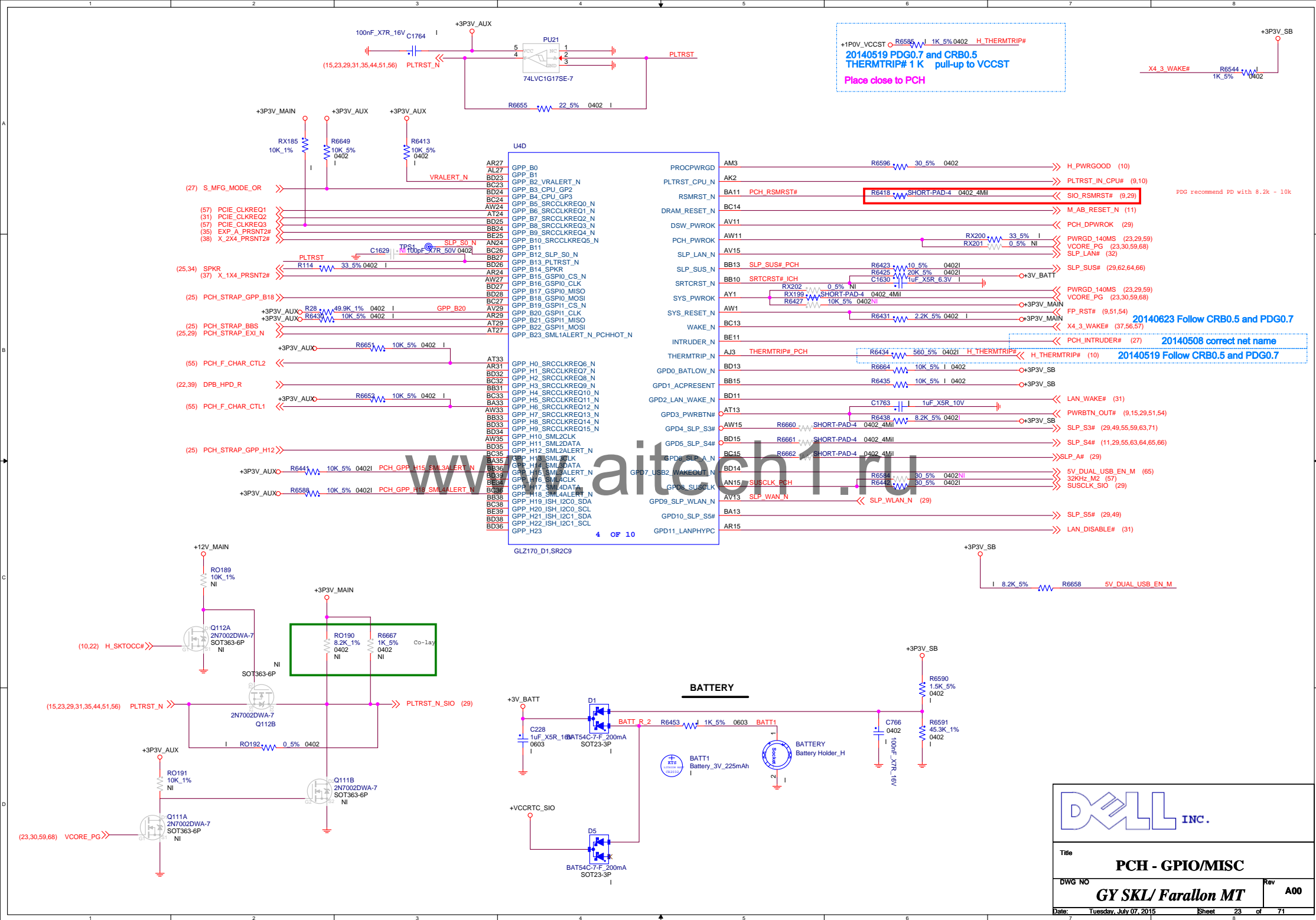
USB3 and USB2 port mapping is not clear in PDG.
Have to check again if Intel releases new PDG.



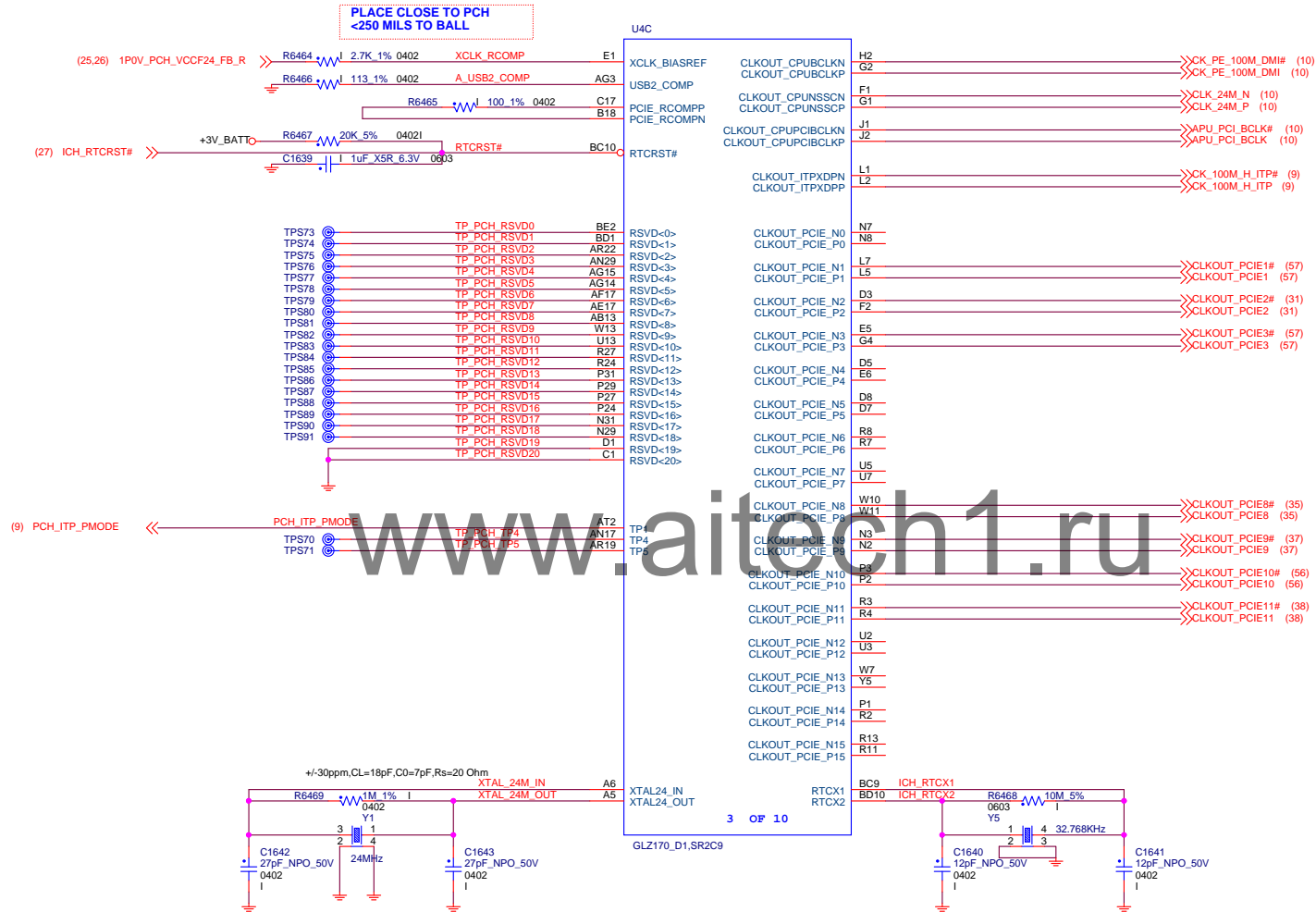


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PCH - CLOCK DISTRIBUTION



M2 for Wifi

Intel LAN PHY Jacksonville.

M2 for SSD

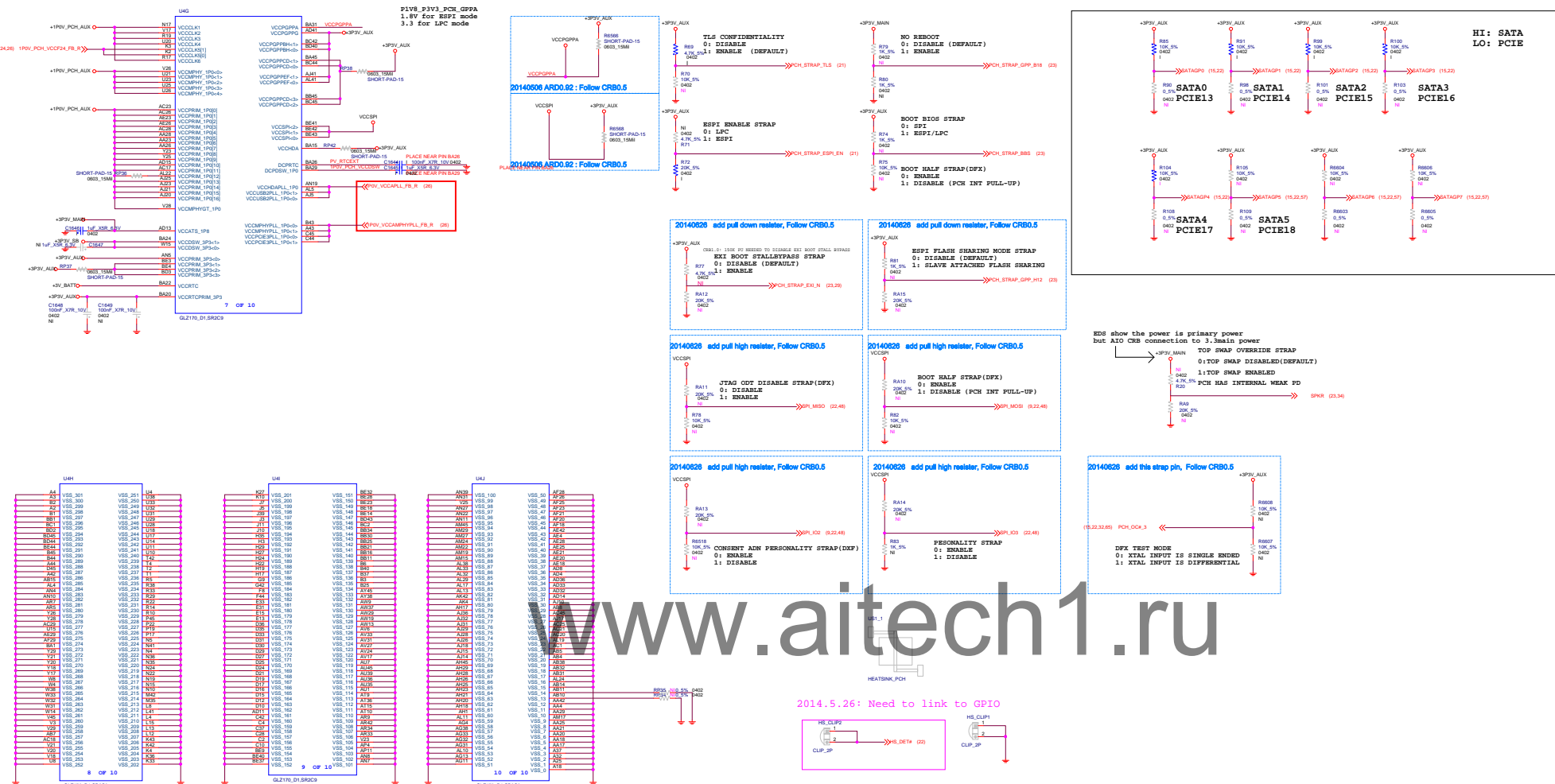
For PCIe X16 Slot

PCI EXPRESS x 4 SLOT 3

For PCIe to PCI bridge

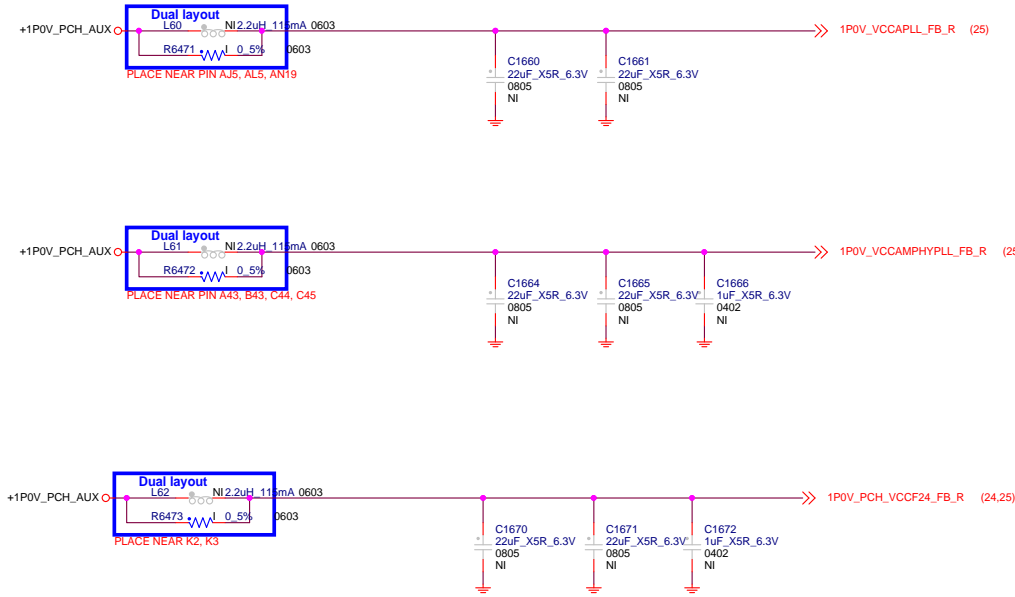
PCI EXPRESS x 4 SLOT 4



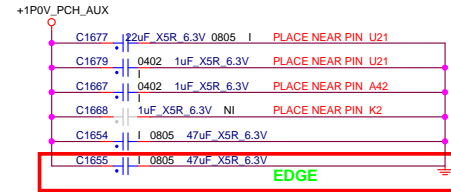


SKYLAKE Decoupling & filter

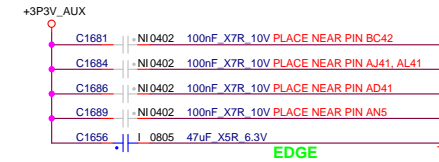
FILTER



V1.0A



V1.8A / V3.3A



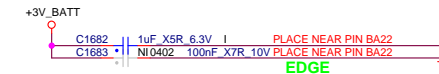
V1.8A / V1.8S / V3.3S



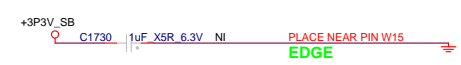
V3.3A



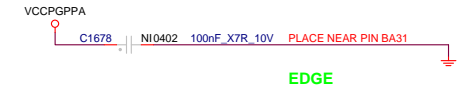
VCCRTC



V3.3 DSW



VccPGPPA



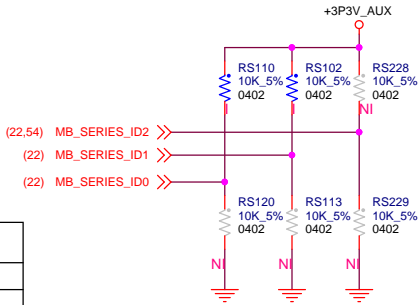
Power Plane Isolation

Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

MB series ID

ID1	ID0	Type
0	0	SFF3
0	1	SFF7
1	0	SFF9
1	1	Farallon

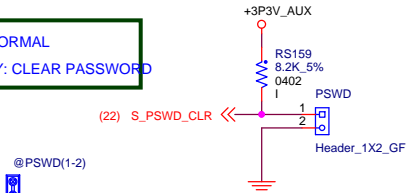


Clear Password

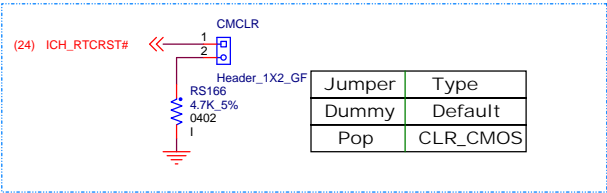
1-2: NORMAL
EMPTY: CLEAR PASSWORD

@PSWD(1-2)

Jumper_2P_GF_Blue

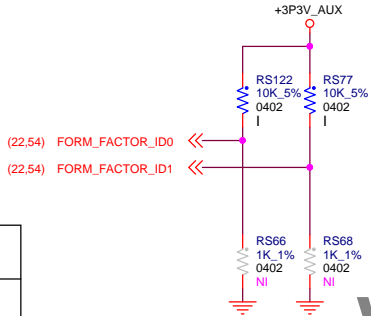


CLR_CMOS

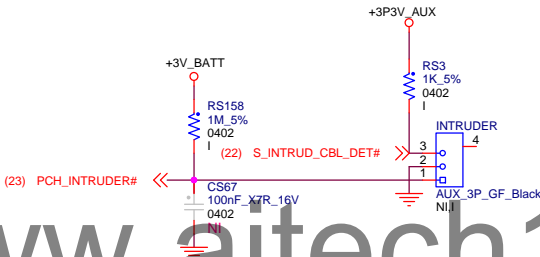


Form Factor ID

ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro

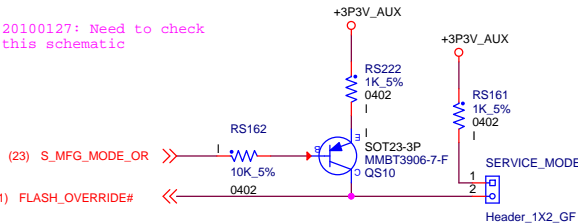


Chassis Intruder



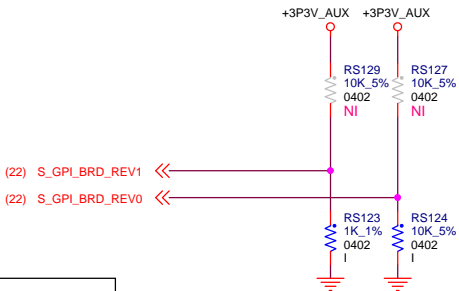
ME Disable (Flash override)

20100127: Need to check
this schematic



BOARD ID

ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00



BEEP



Title
PCH-8:MISC CONN/BEEP/ID

DWG NO
GY SKL/ Farallon MT

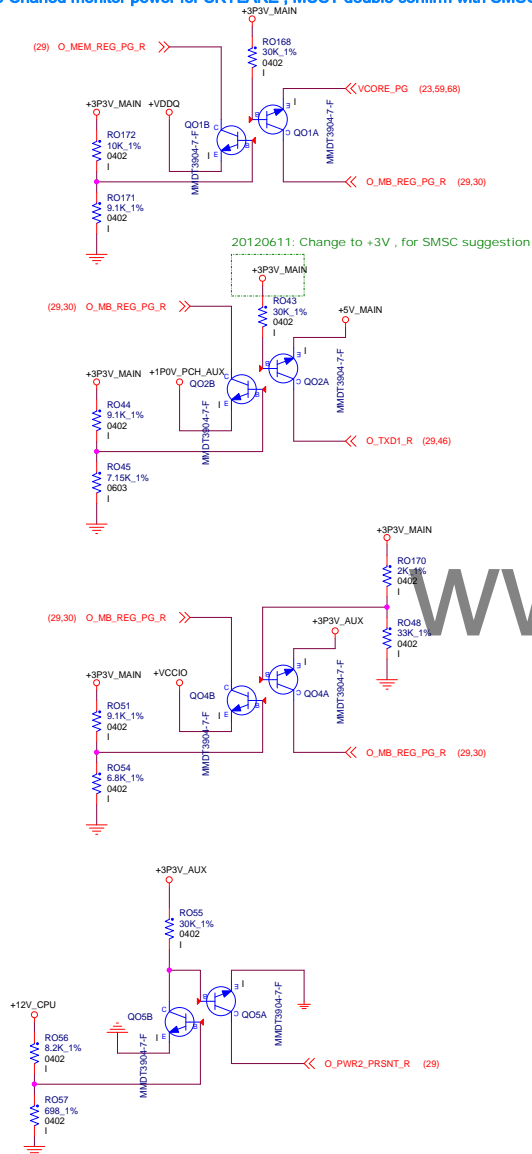
Date: Tuesday, July 07, 2015 Sheet 27 of 71



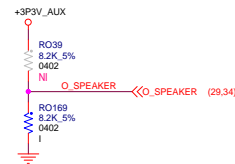
www.aitech1.ru

5555 PRE-POST DIAG Monitor

20140429 Chaned monitor power for SKYLAKE , MUST double confirm with SMSC



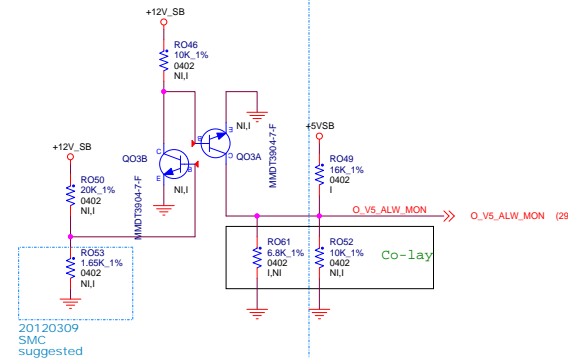
SIO STRAPING



SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

SIO5555 V5_ALW Monitor



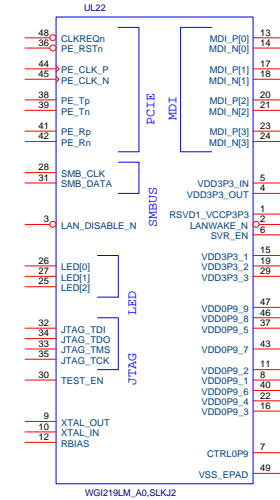
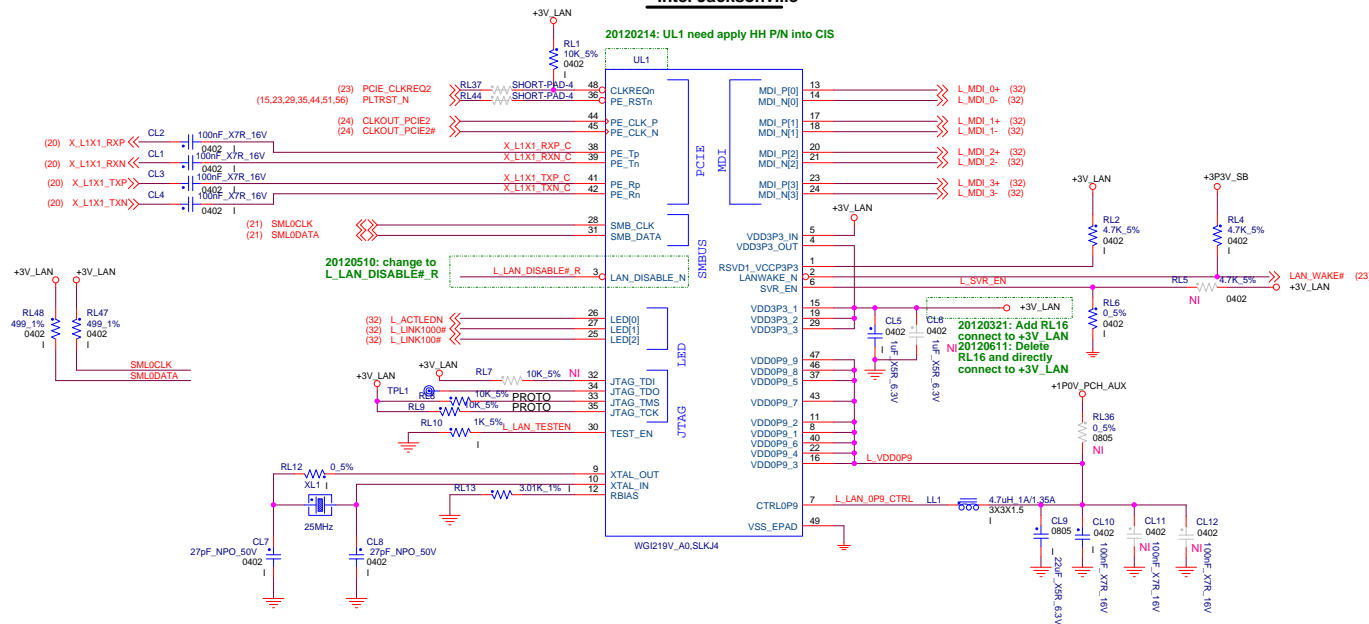
For single Power ONLY



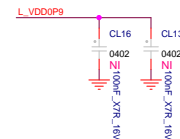
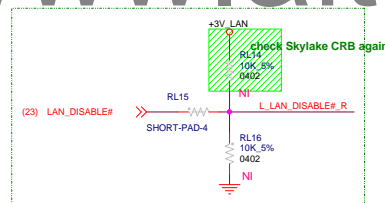
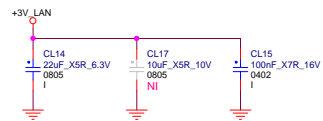
Jacksonville need applied CIS.

Intel Jacksonville

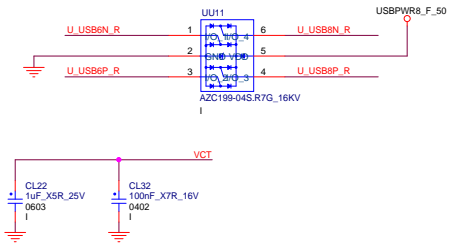
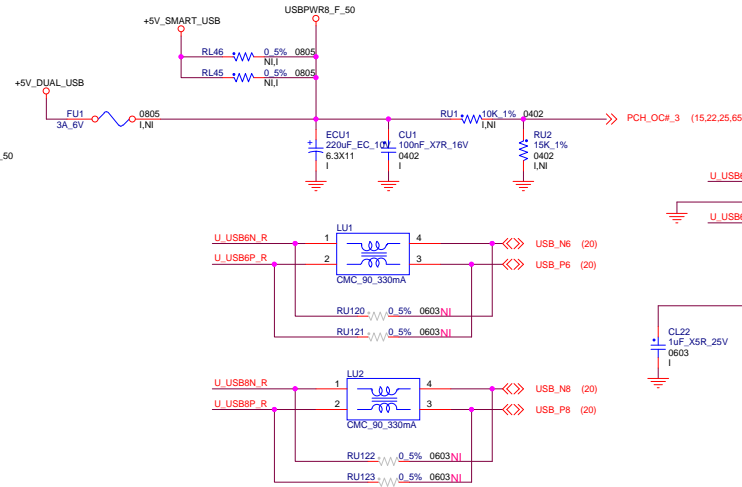
20120214: UL1 need apply HH P/N into CIS



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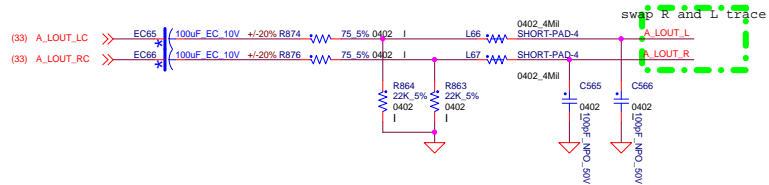
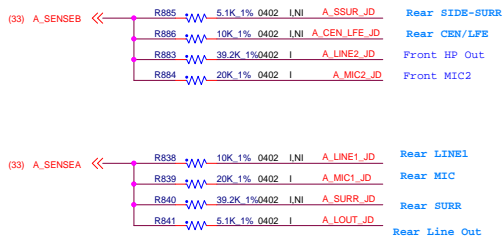


LED's:
10MHz : OFF
100MHz: Yellow
1GHz : Green

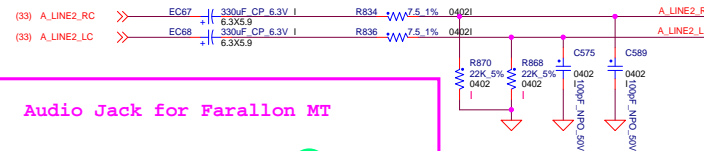
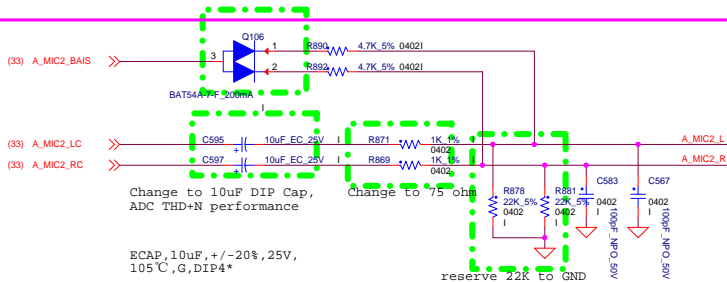
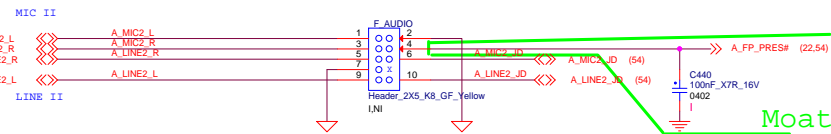


A circuit diagram showing a 1uF capacitor (labeled CL28, 1uF_X5R_16V, 0603) connected between a +3P3V_SB power source and ground.

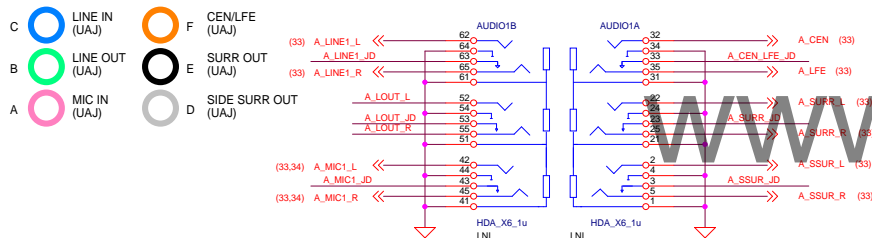
JACK SENSE



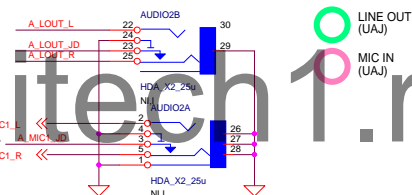
Front_Audio for Good Year SKL



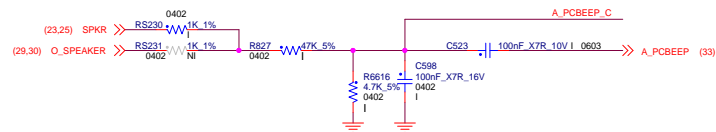
Audio Jack for GOODYEAR SKL



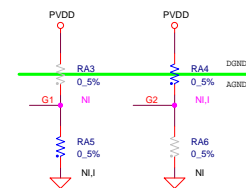
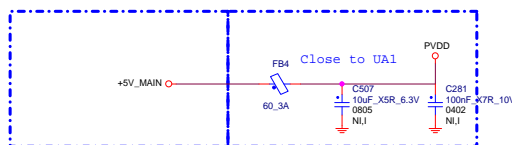
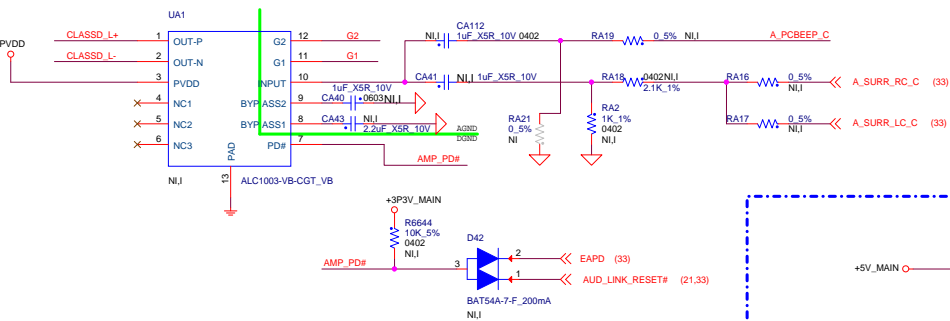
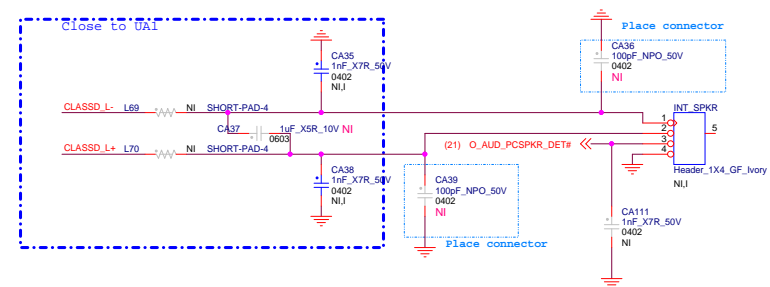
Audio Jack for Farallon MT

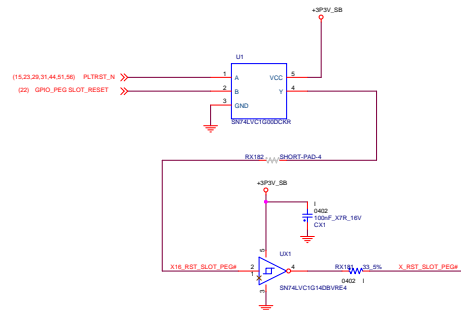
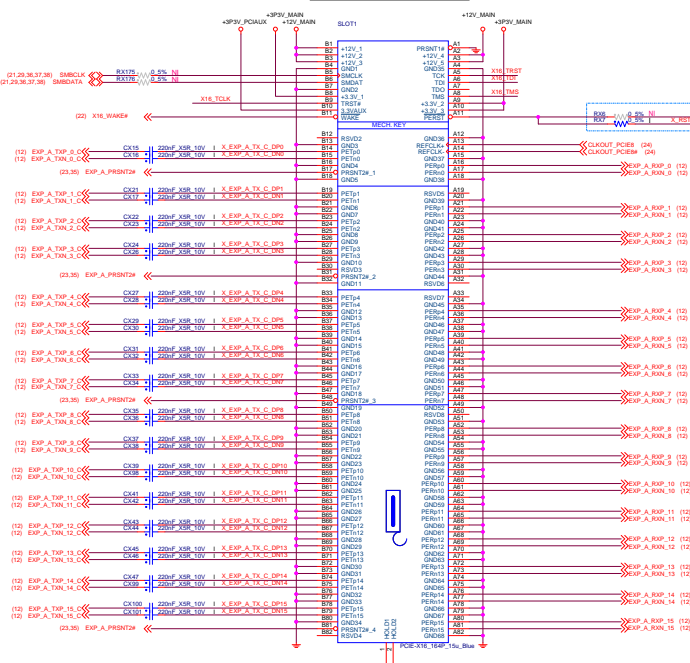


PC BEEP

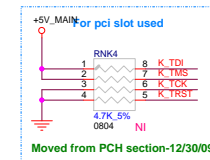
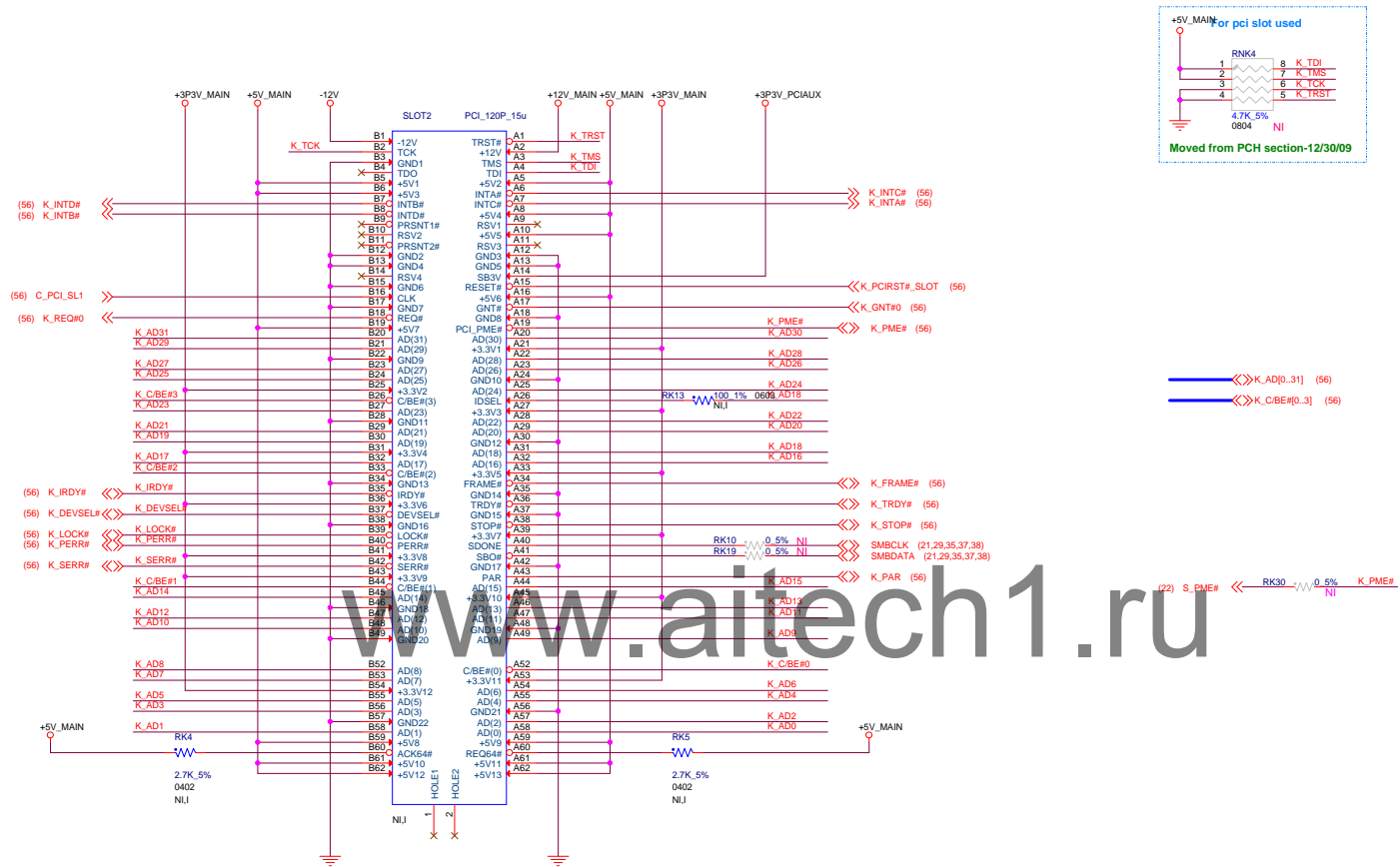


CHASSIS SPEAKER for Farallon MT



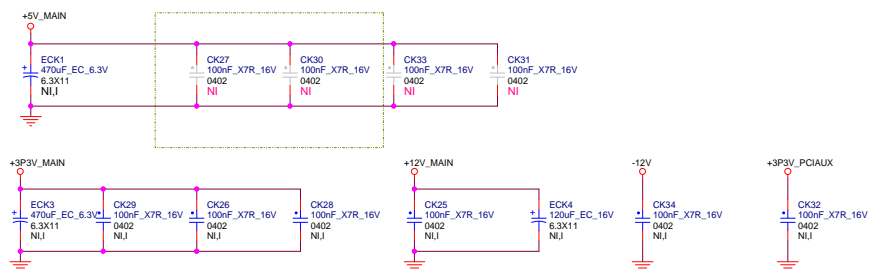


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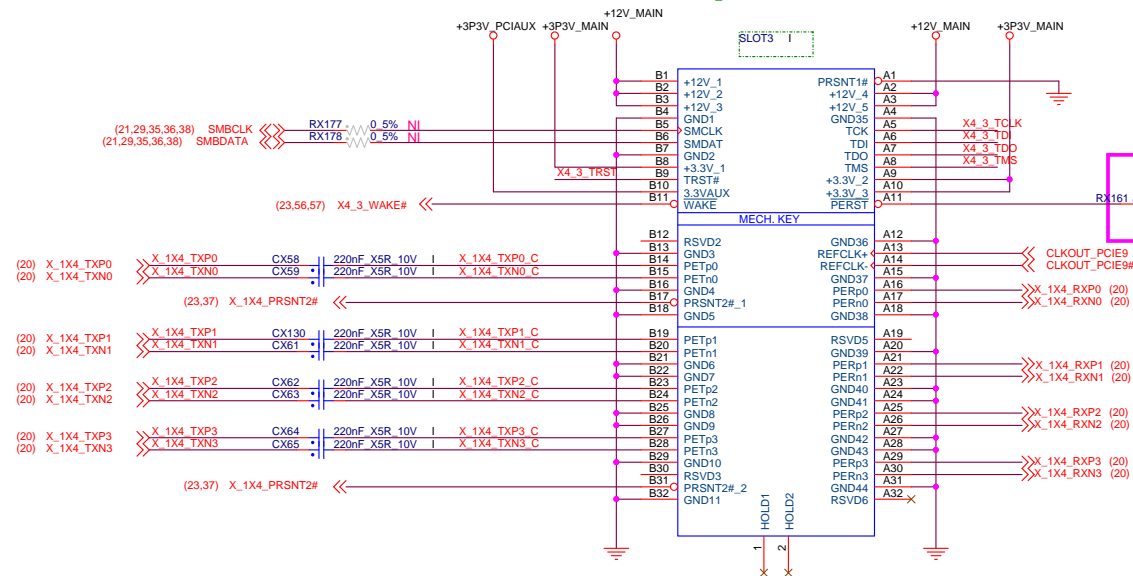


<<< K.AD[0..31] (56)
 <<< K.CBE#[0..3] (56)

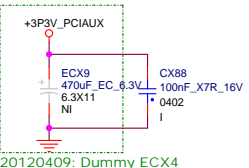
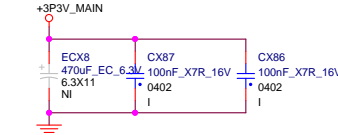
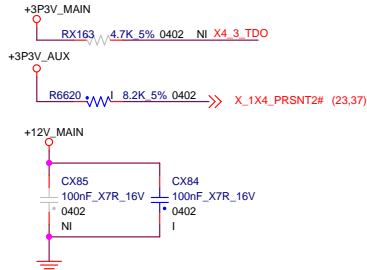
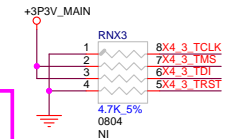
(22) S.DME# <<< RK30 0.5% NI K.PME#



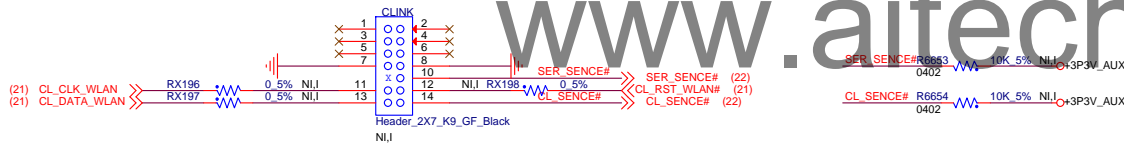
20120315: SLOT1 change to 15u" parts
FOXCONN_2EG03217-22DB-DF



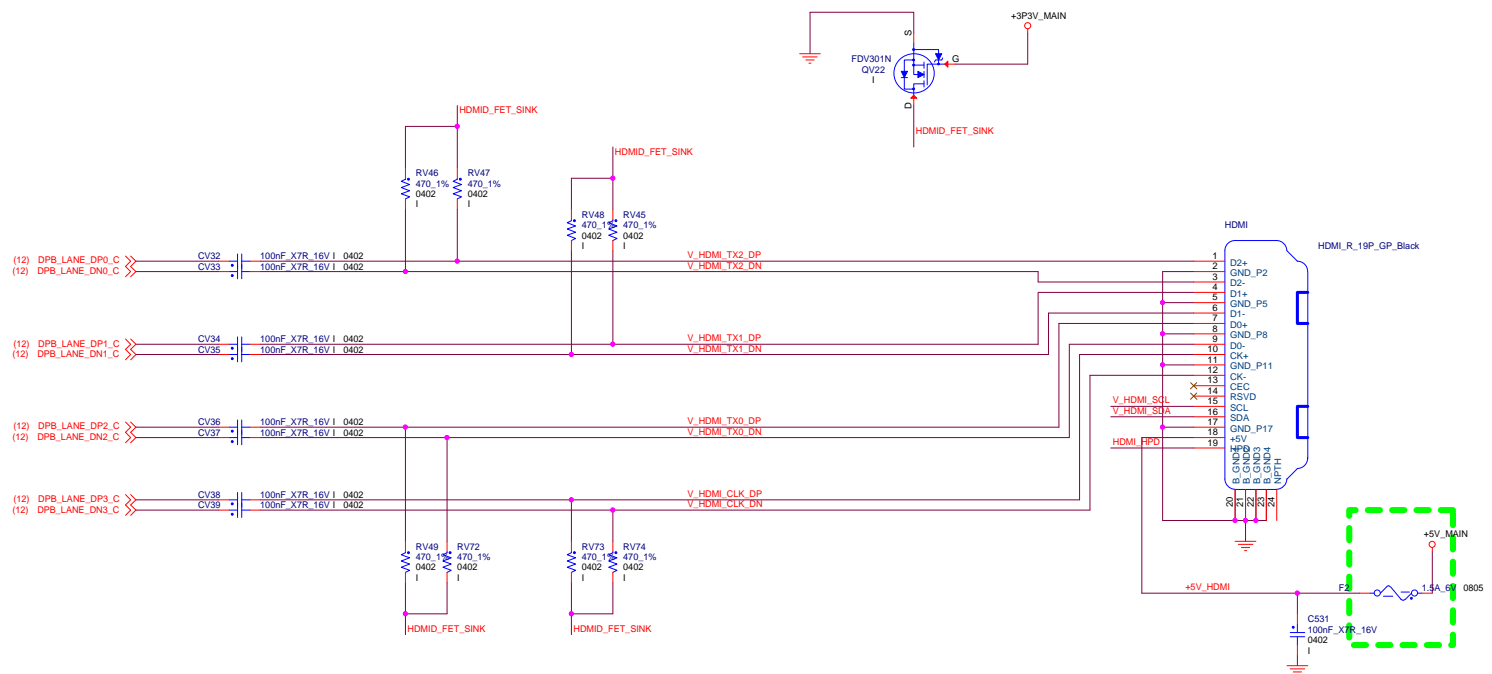
Check Slot 3&4 PCIe reset logic



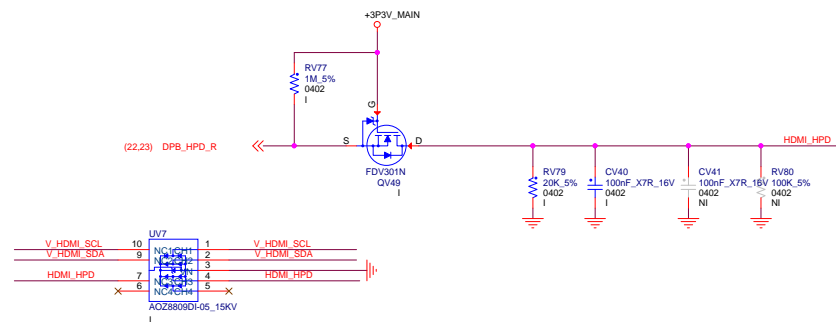
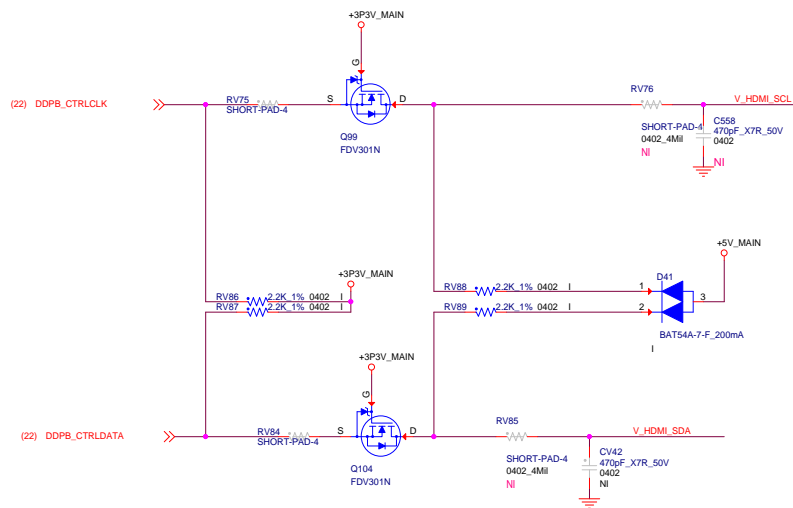
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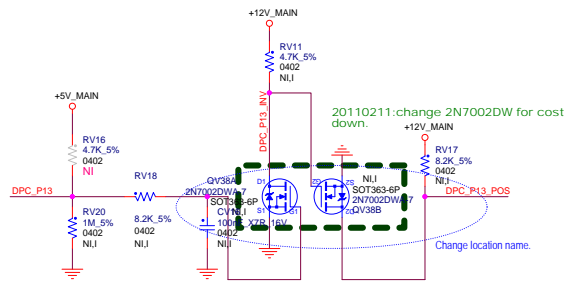
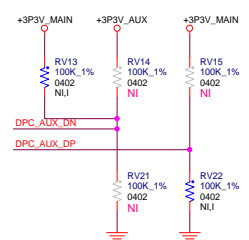
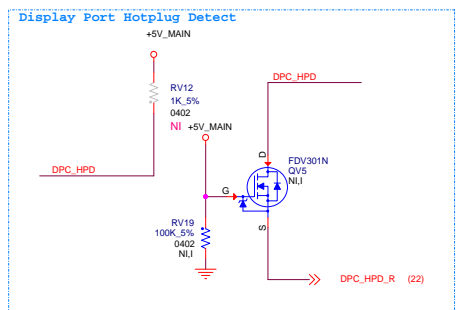
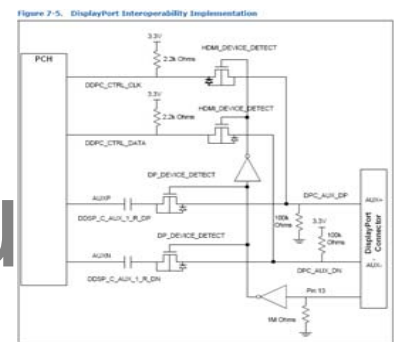
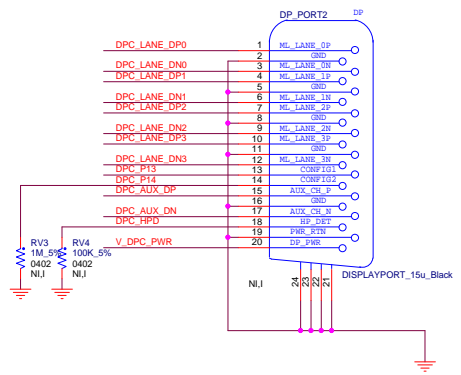
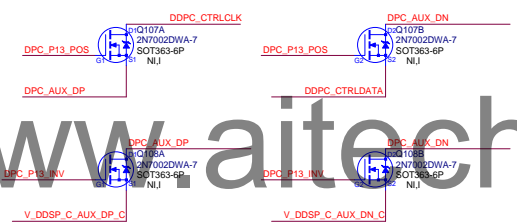
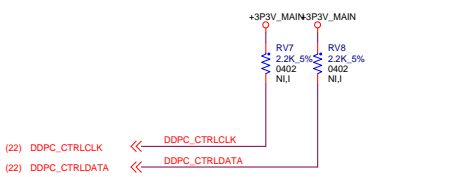
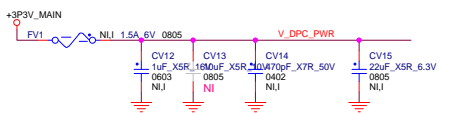
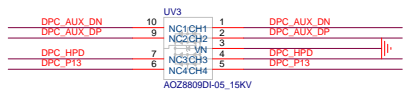
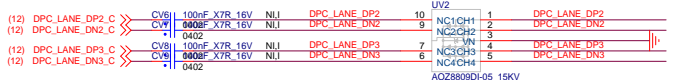


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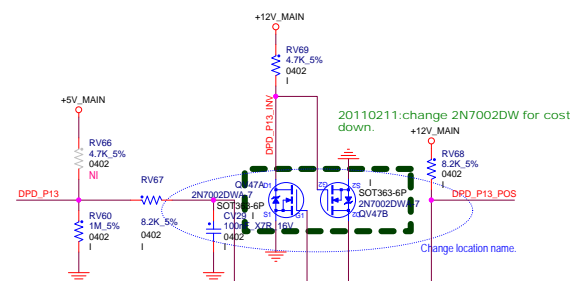
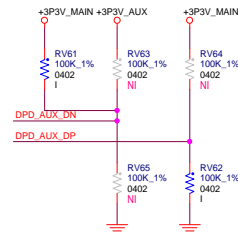
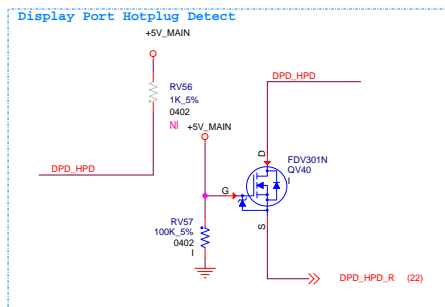
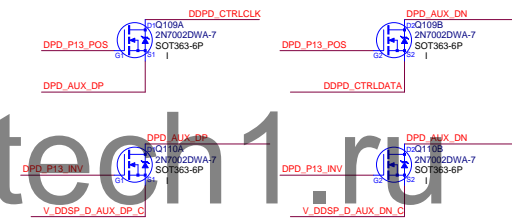
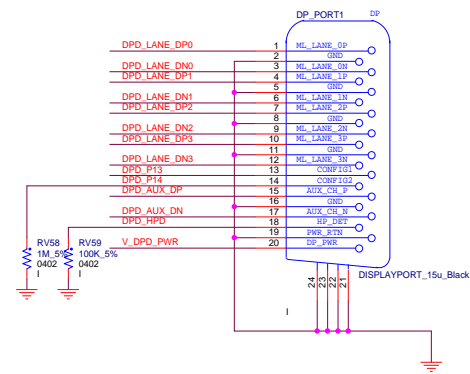
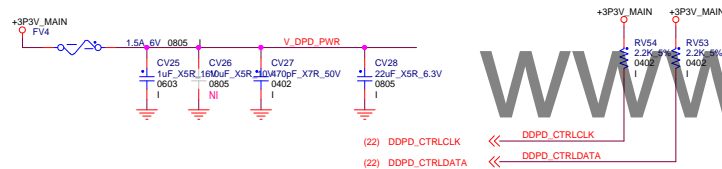
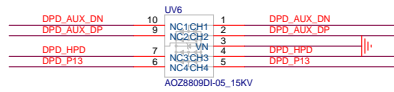
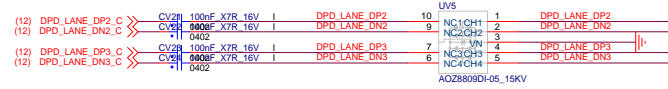
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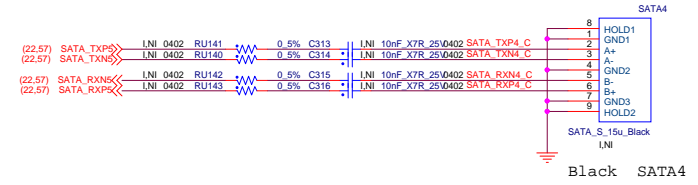
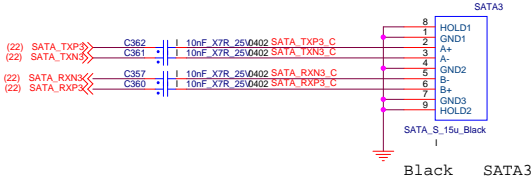
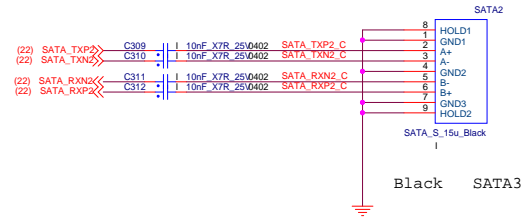
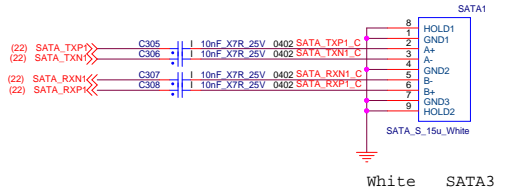
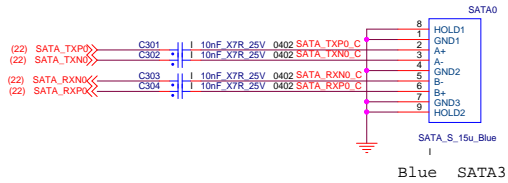
[illegible]

(1)	DPO_LANE_DP0_C	CV1H	100nF	X7R	16V	I		DPO_LANE_DP0	10	UV4	1	DPO_LANE_DP0
(12)	DPO_LANE_DN0_C	CV1H	0000F	X7R	16V	I		DPO_LANE_DN0	9	N1C1GH	2	DPO_LANE_DN0
		+*	0402							N2C2GH	3	
(1)	DPO_LANE_DP1_C	CV1H	100nF	X7R	16V	I		DPO_LANE_DP1	7		4	DPO_LANE_DP1
(12)	DPO_LANE_DN1_C	CV1H	0000F	X7R	16V	I		DPO_LANE_DN1	6	N3C3GH	5	DPO_LANE_DN1
		+*	0402							N4C4GH	6	

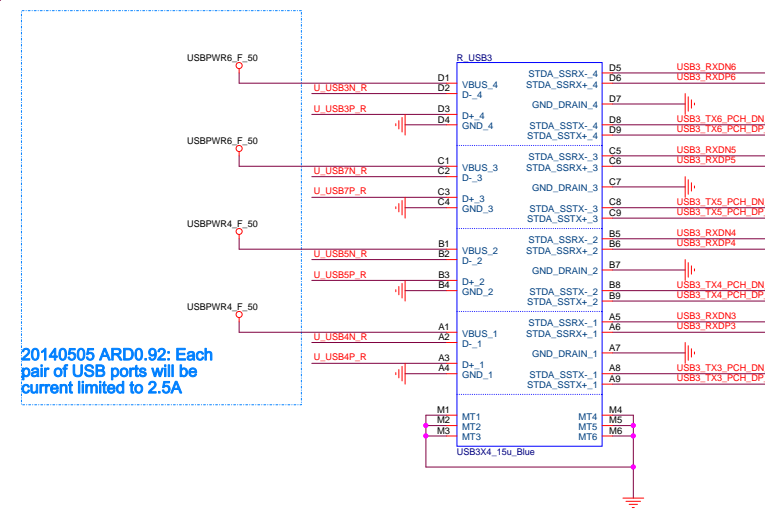
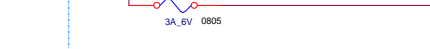
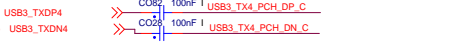
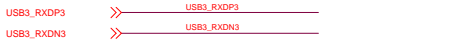
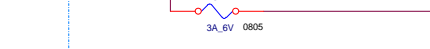
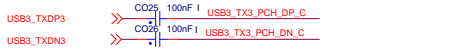
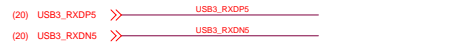
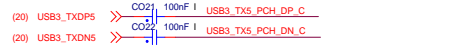
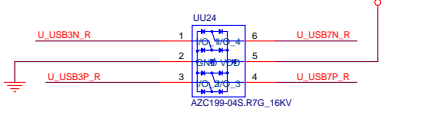
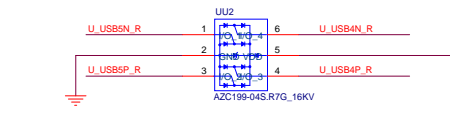
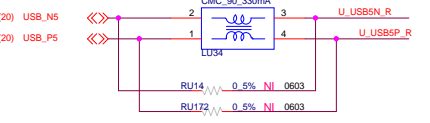
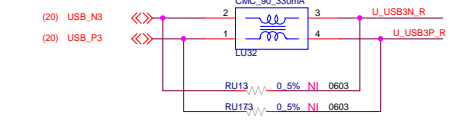
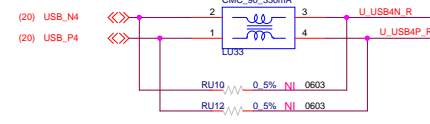
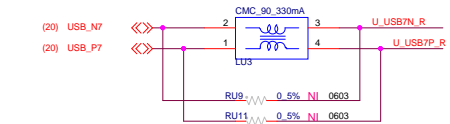
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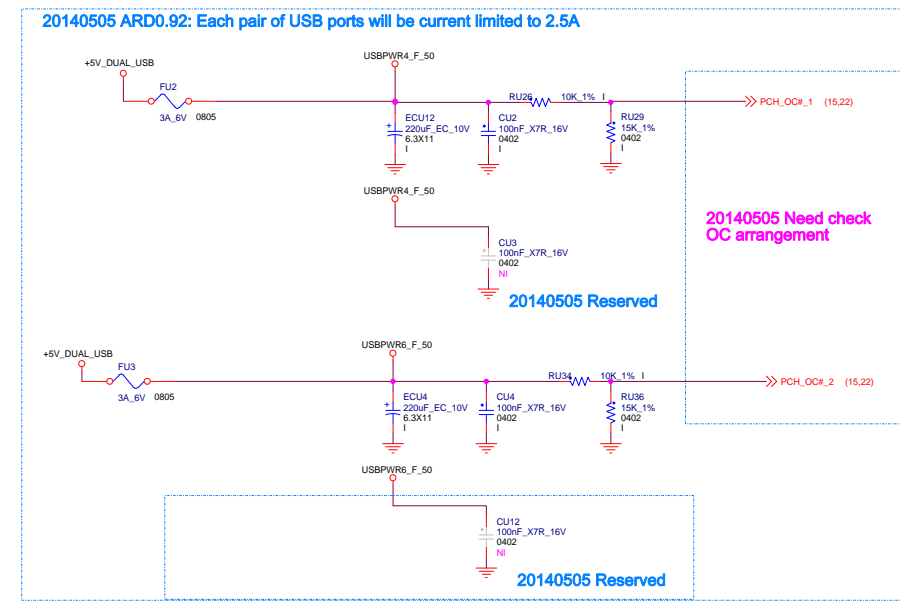
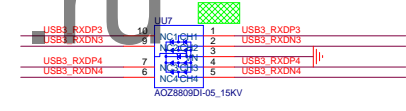
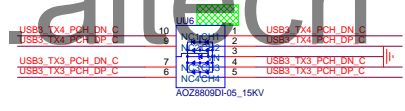
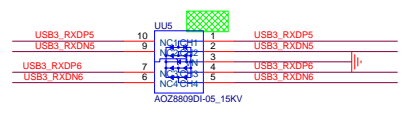
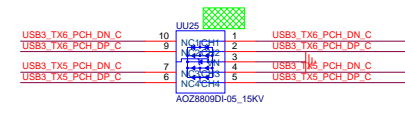
DARK BLUE



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Place ESD Close to Connector



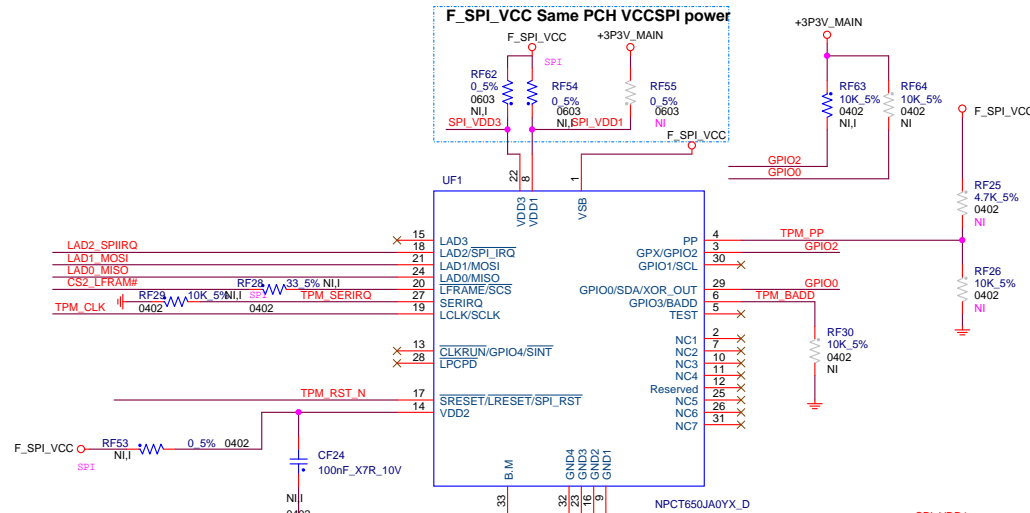
20140505 Need check OC arrangement

20140505 Reserved

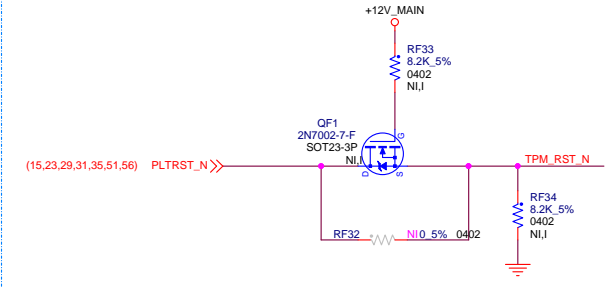
20140505 Reserved

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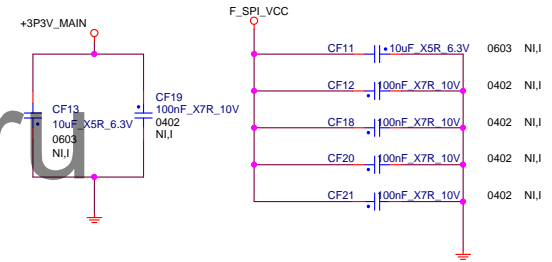
Nuvoton NPCT650JAAYX



20140508 Follow Dell D serials design

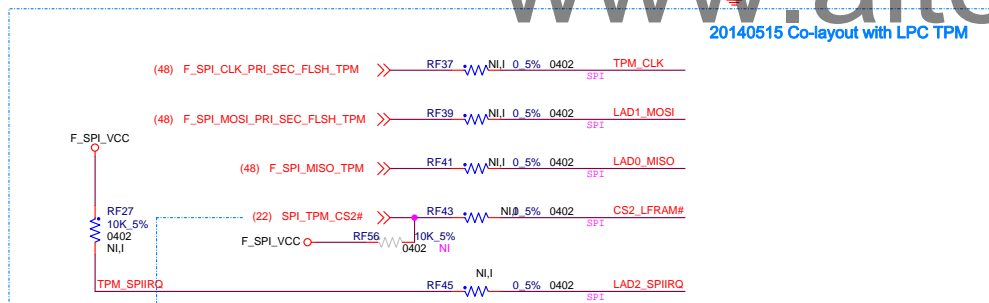


Decoupling Capacitors

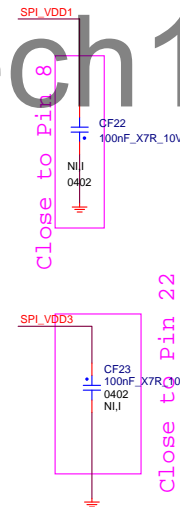


NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.

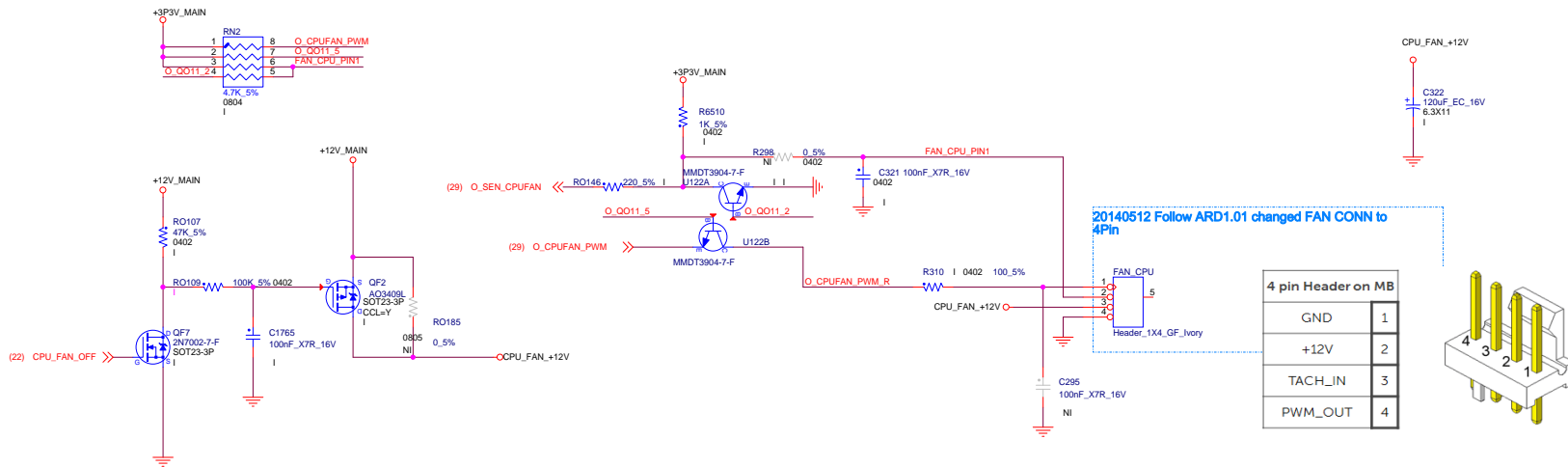
20140515 Co-layout with LPC TPM



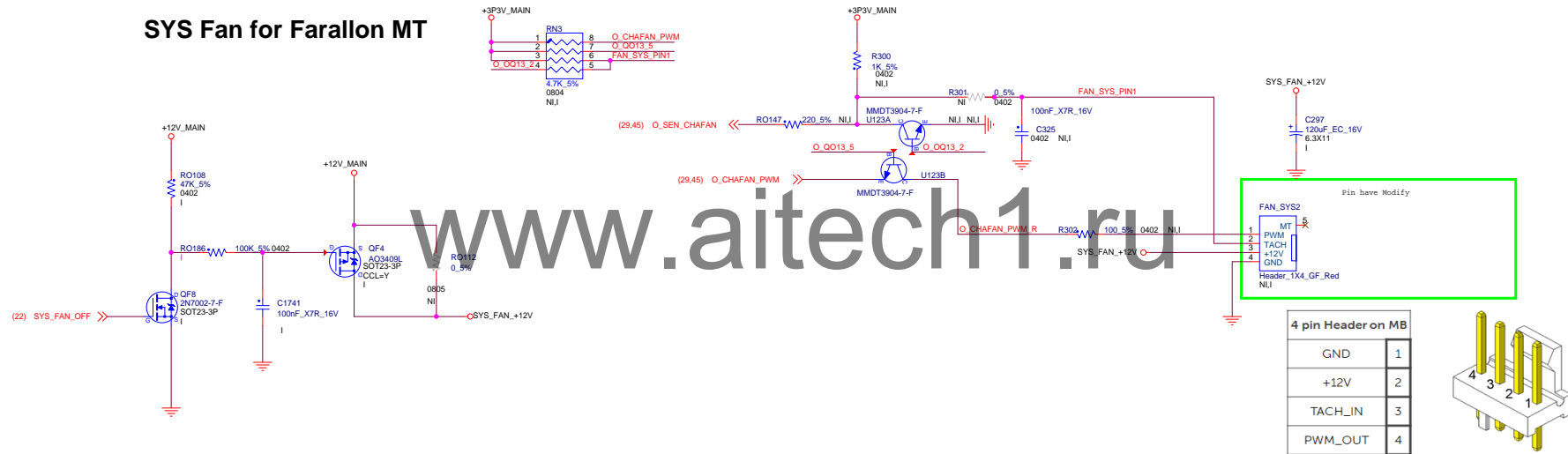
20140509 Changed net name to SPI_TPM_CS2#



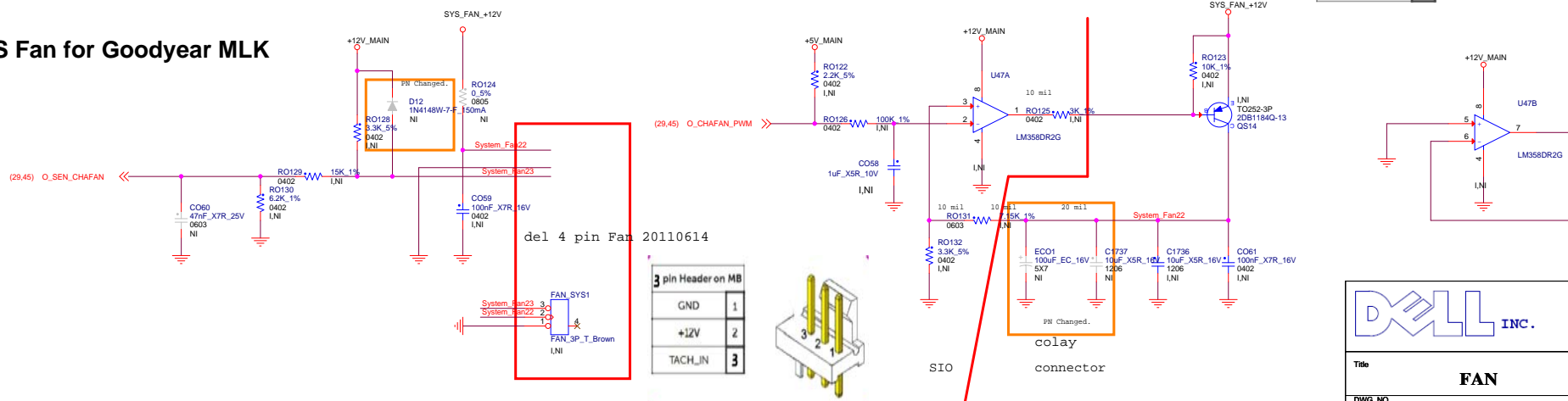
CPU Fan



SYS Fan for Farallon MT

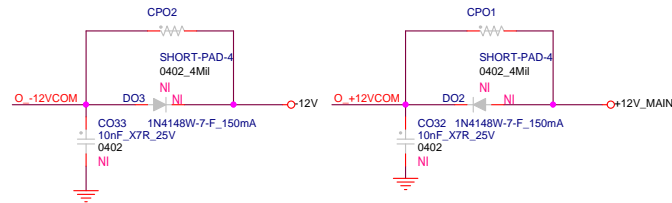
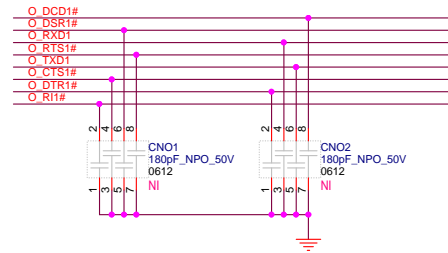
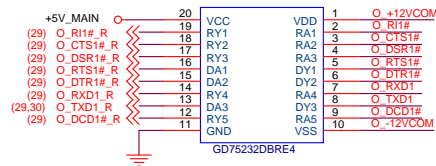


SYS Fan for Goodyear MLK

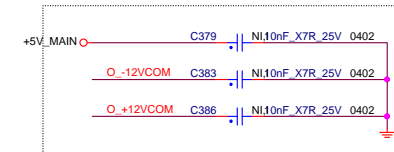
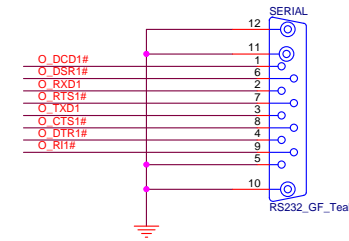


SERIAL A

12V solution



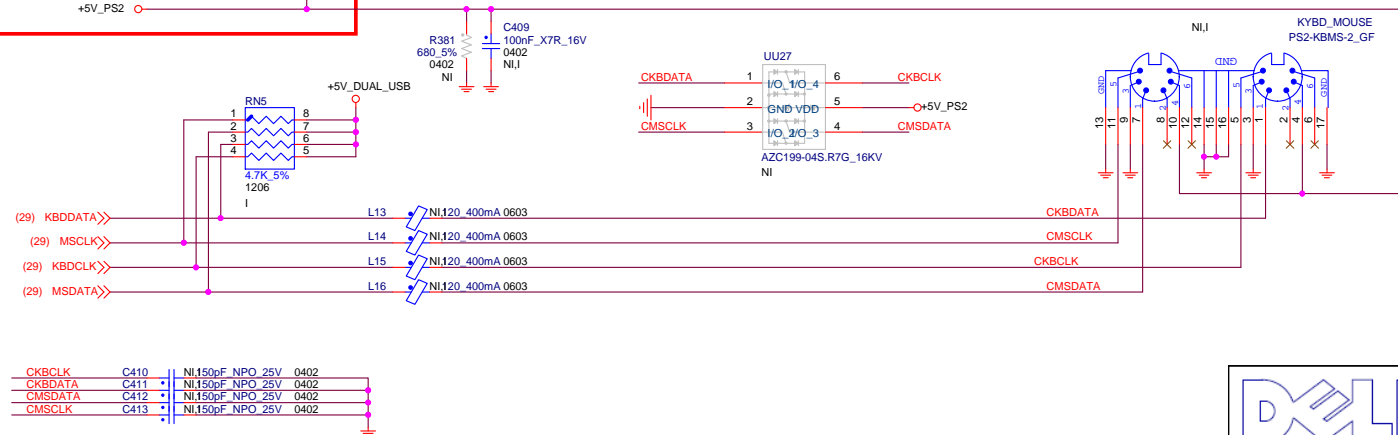
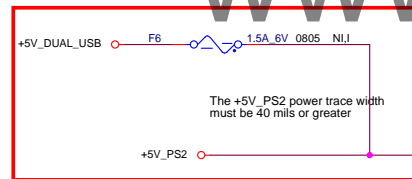
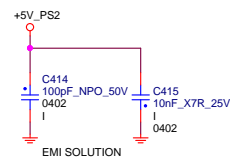
SERIAL B



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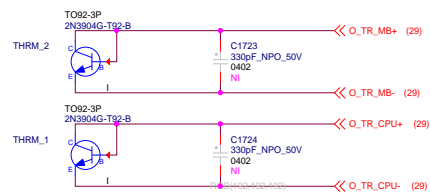
PS2 KEYBOARD / MOUSE

Change BOM option.



DELL INC.	
Title	COM/PS2
DWG NO	GY SKL/ Farallon MT
Date: Tuesday, July 07, 2015	Rev A00
Sheet 46	of 71

Thermal Header



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Title

TBD

DWG NO

GY SKL/ Farallon MT

Rev

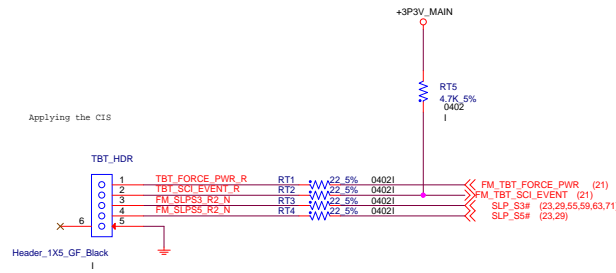
A00

Date: Tuesday, July 07, 2015

Sheet 47 of 71

TBT

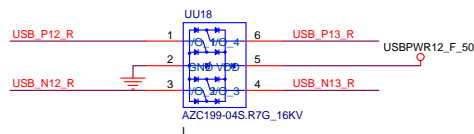
Applying the CIS



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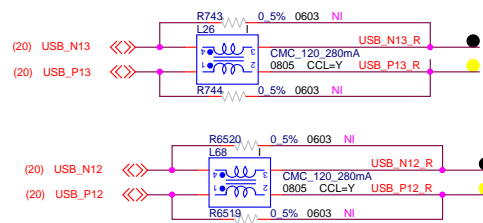
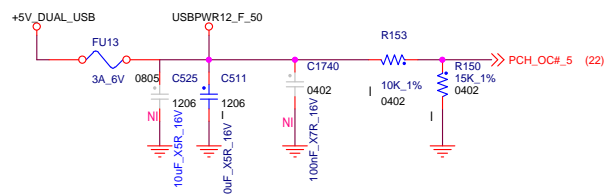


Title		Rev
TBT_HDR		A00
DWG NO	GY SKL/ Farallon MT	
Date: Tuesday, July 07, 2015	Sheet	49 of 71



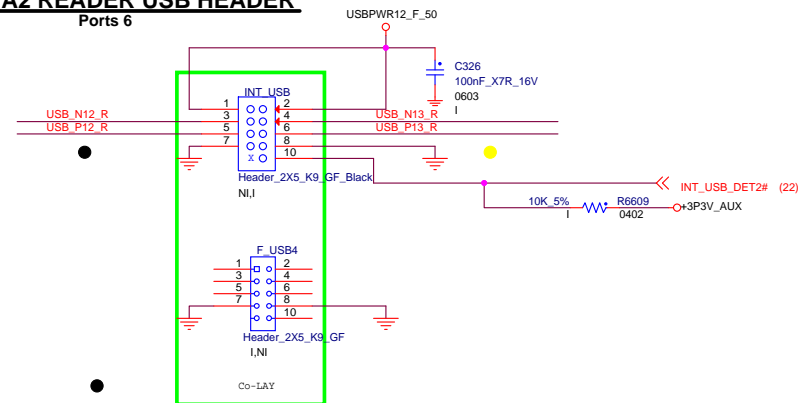
Place ESD Close to Header

USB2.0



MEDIA2 READER USB HEADER

Ports 6

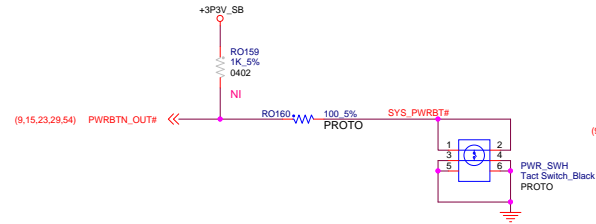


GY SKL F_USB4 Card reader Black color

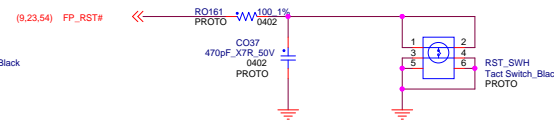
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DELL INC.	
Title	BLANK
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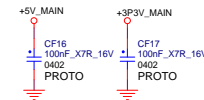
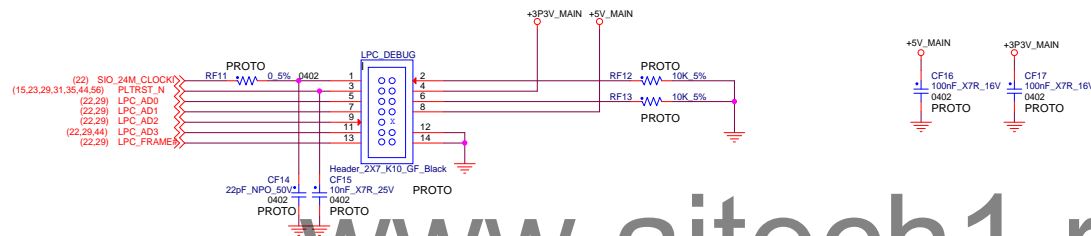
Power Bottom



Reset Bottom



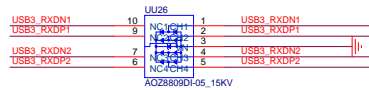
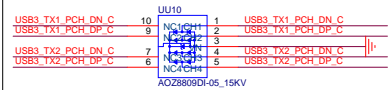
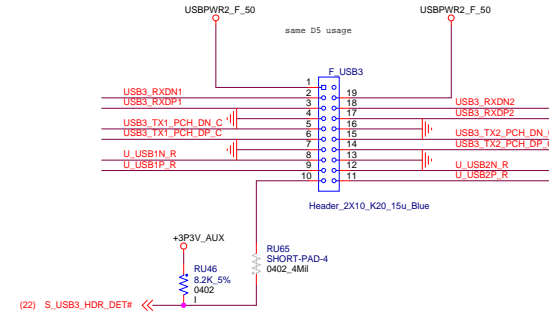
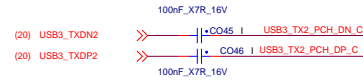
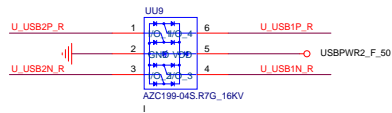
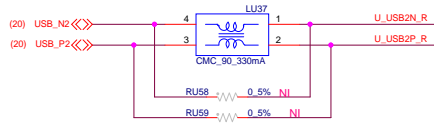
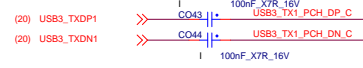
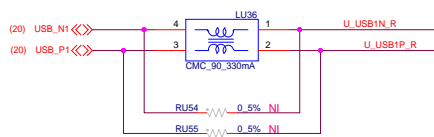
LPC DEBUG



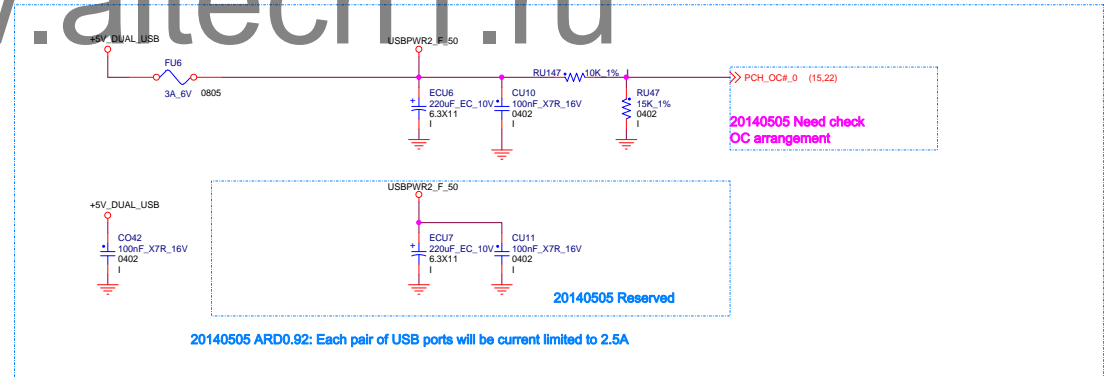
APS Debug

Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_53#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_54#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7	Unused	
Pin 8	GND	Ground
Pin 9	RTCST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

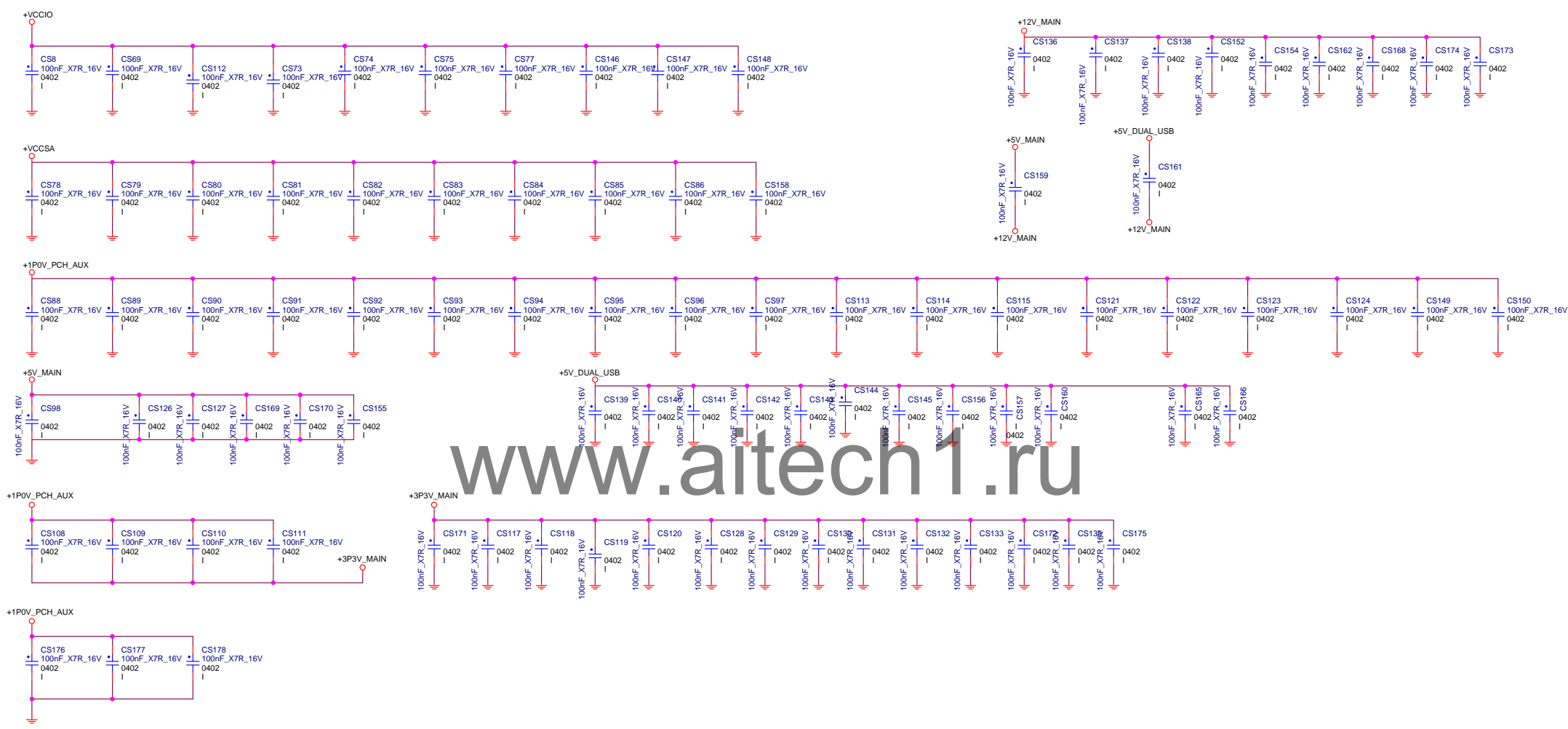




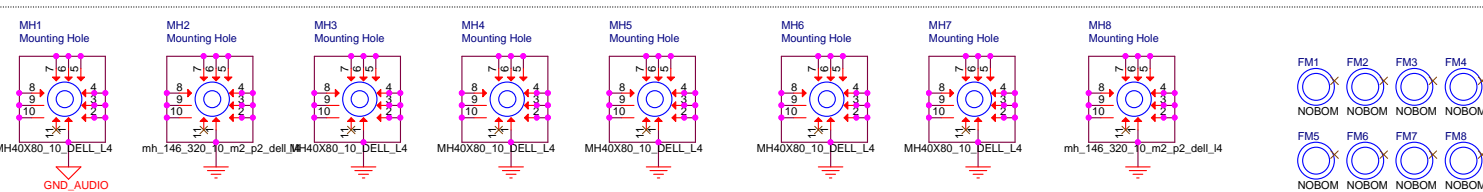
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EMI CAP

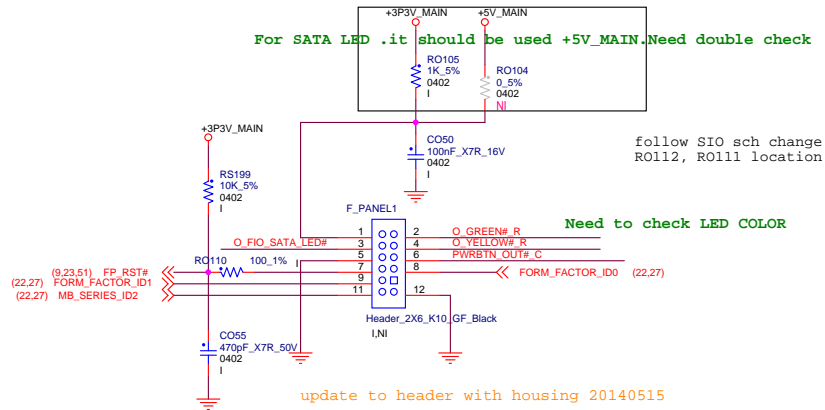


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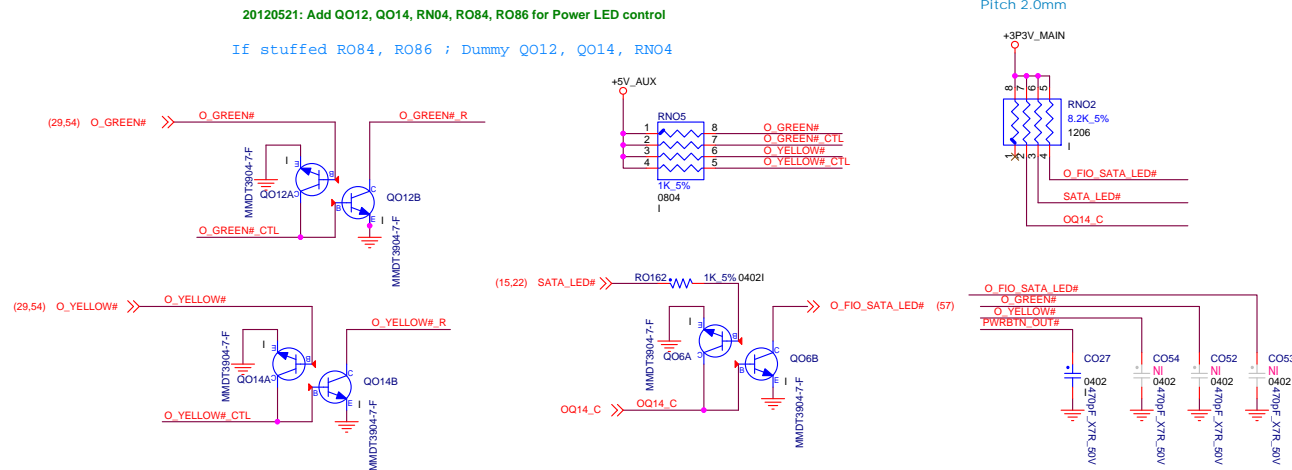
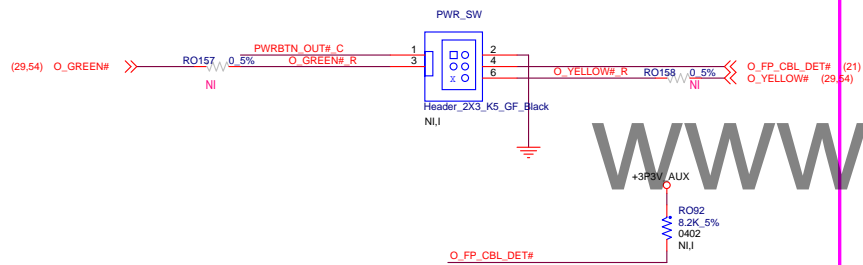


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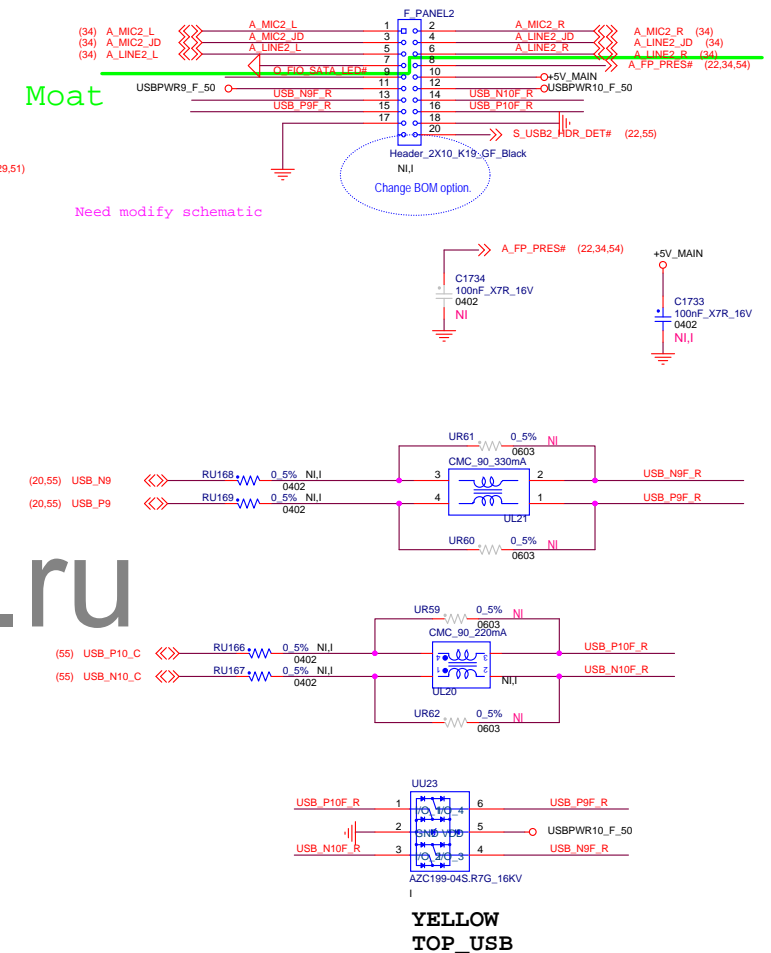
GOODYEAR SKL Front_IO Header



FARALLON MT POWER SWITCH Header

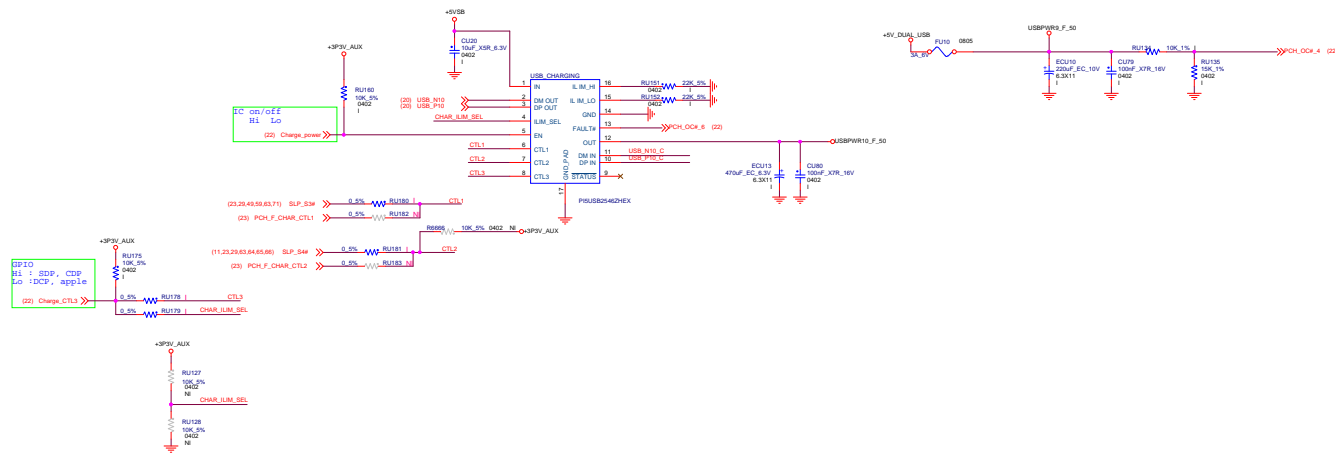


FARALLON MT Front_IO Header

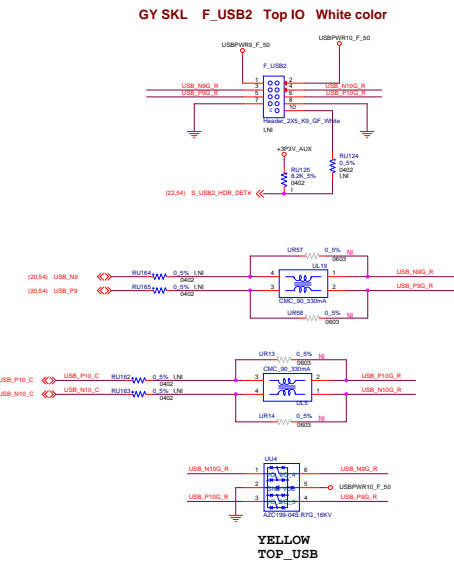


Front Panel		
DWG NO	GY SKL/ Farallon MT	
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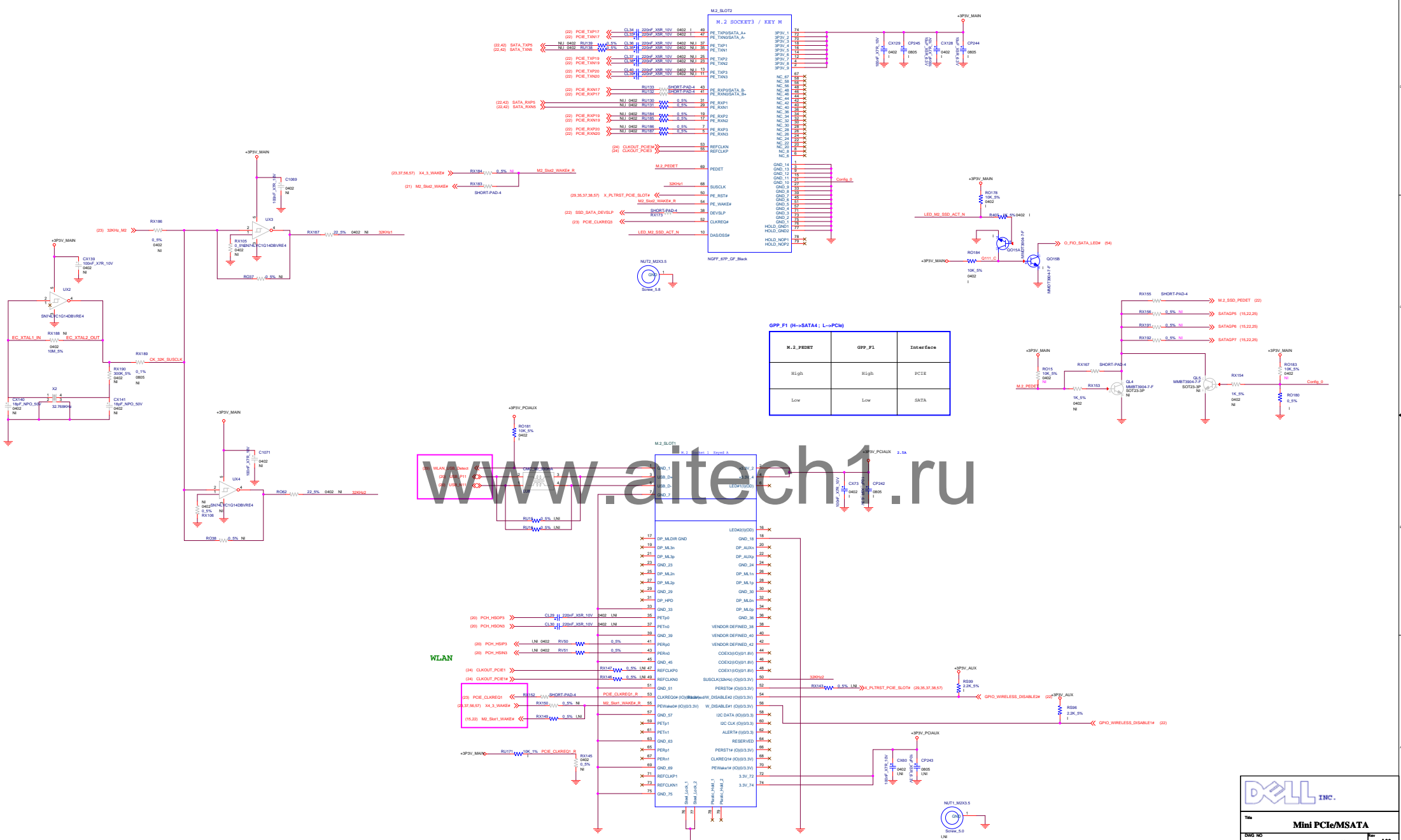
INT USB



Goodyear SKL Front USB



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GPP_F1 (H→SATA4; L→PCIE)		
M.2_PIEDET	GPP_F1	Interface
High	High	PCIe
Low	Low	SATA



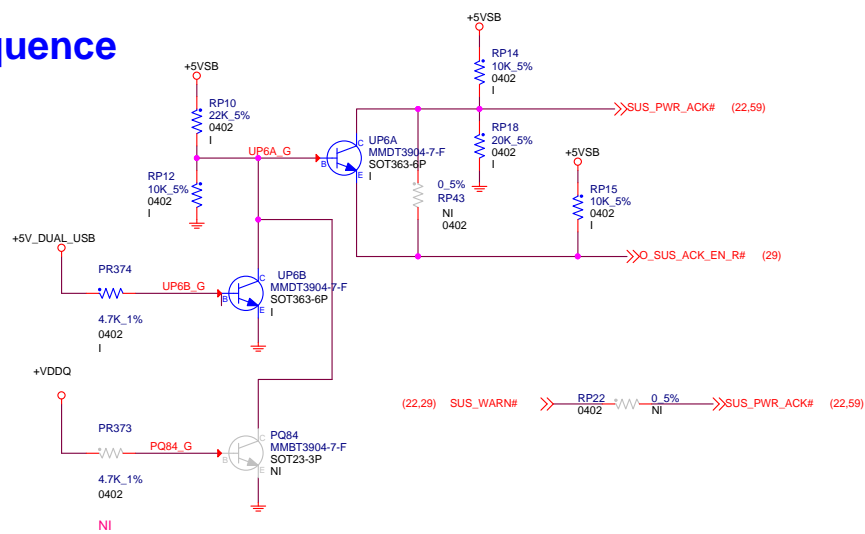
INC.

Mini PCIe/MSATA		
Model	GY SKL / Farallon MT A00	
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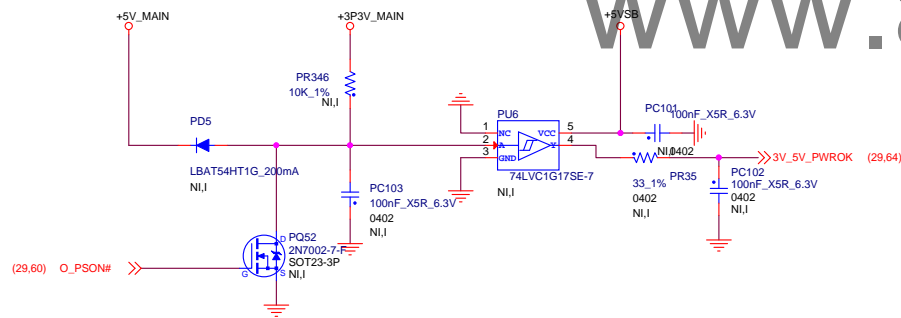
		
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TBD		
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GY SKL/ Farallon MT		
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Power Sequence

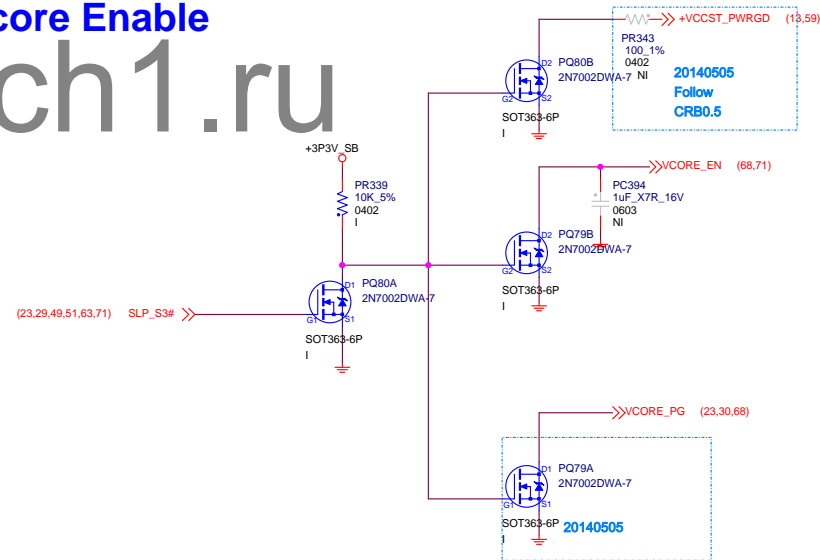


Vcore Enable

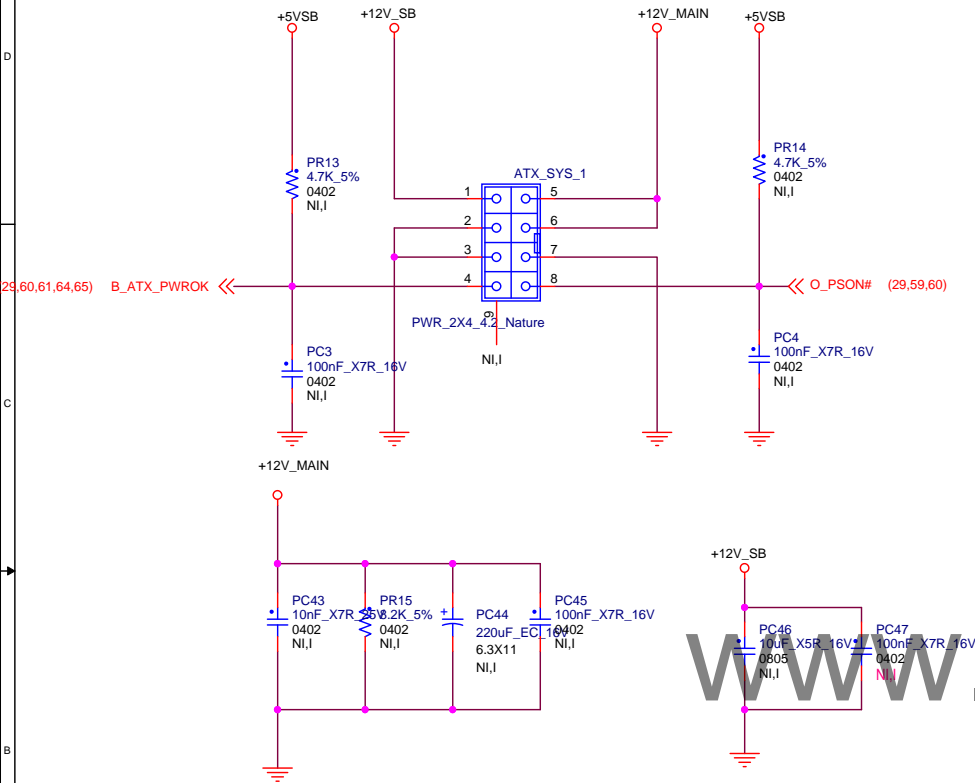
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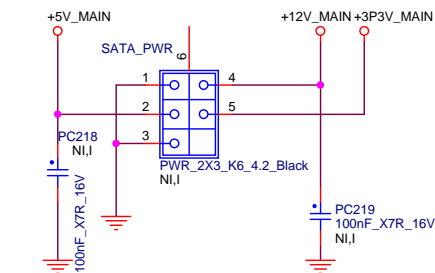
New ATXPWROK



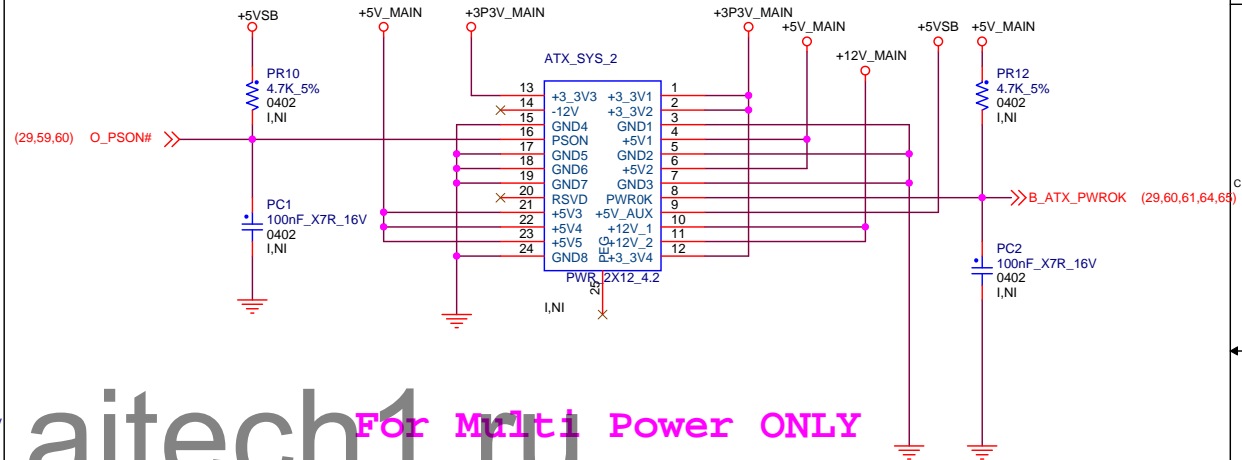
ATX POWER CONNECTOR



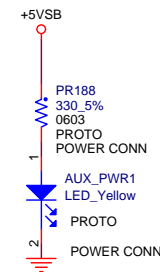
For ODD
and HDD



For single Power ONLY

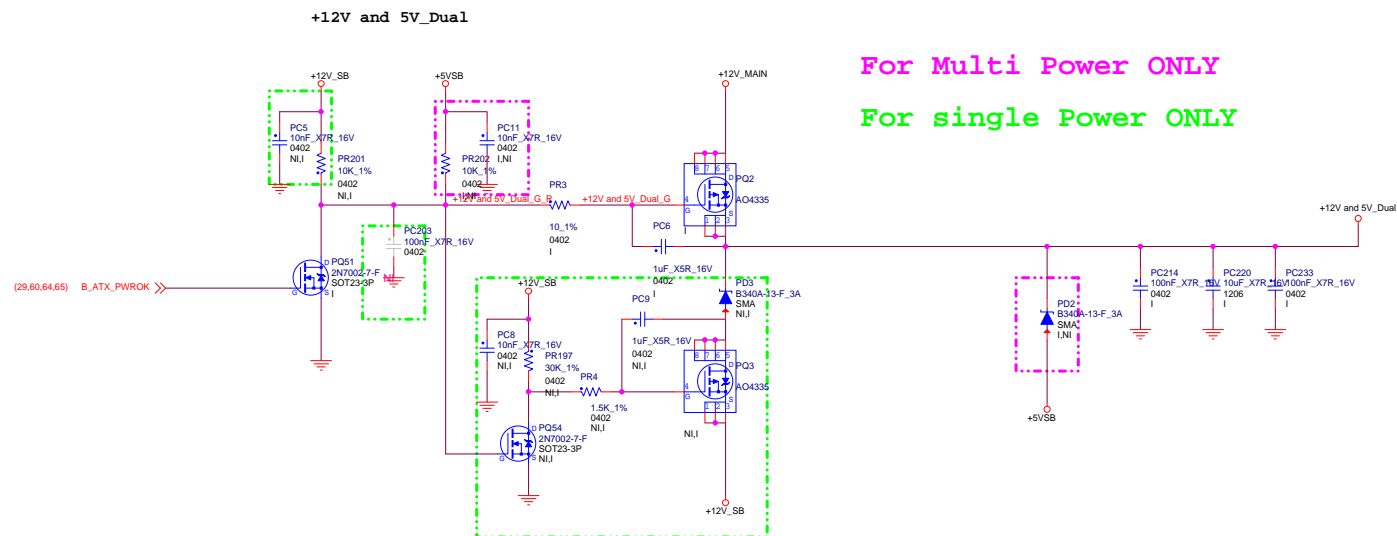


For Multi Power ONLY



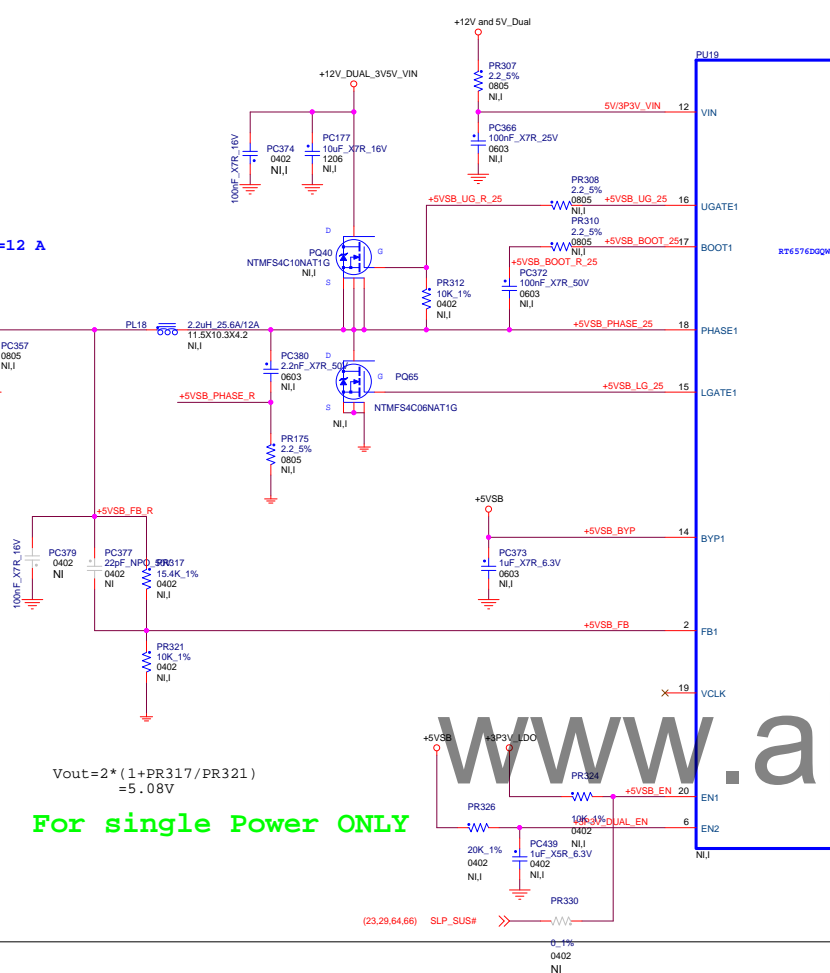
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For Multi Power ONLY
For single Power ONLY



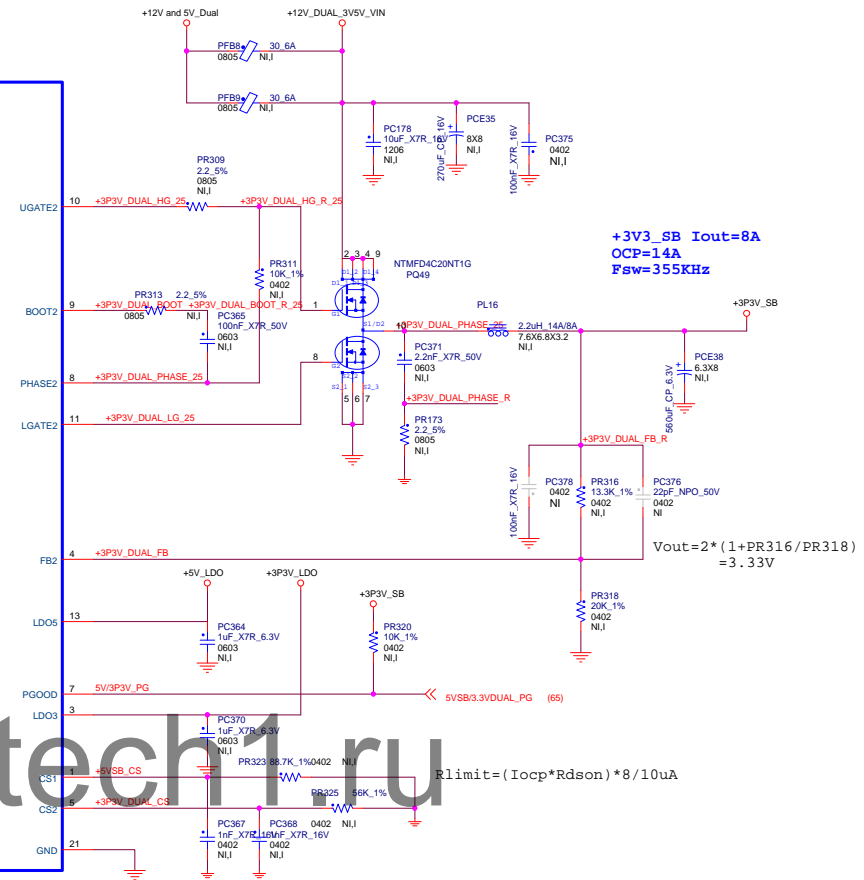
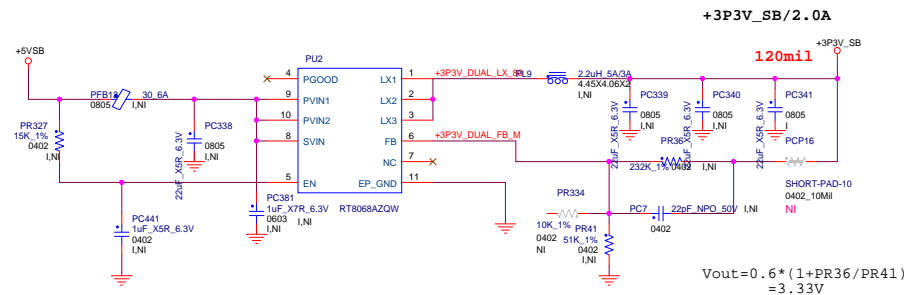
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+5VSB Iout=12 A
OCp=24A
Fsw=300KHz

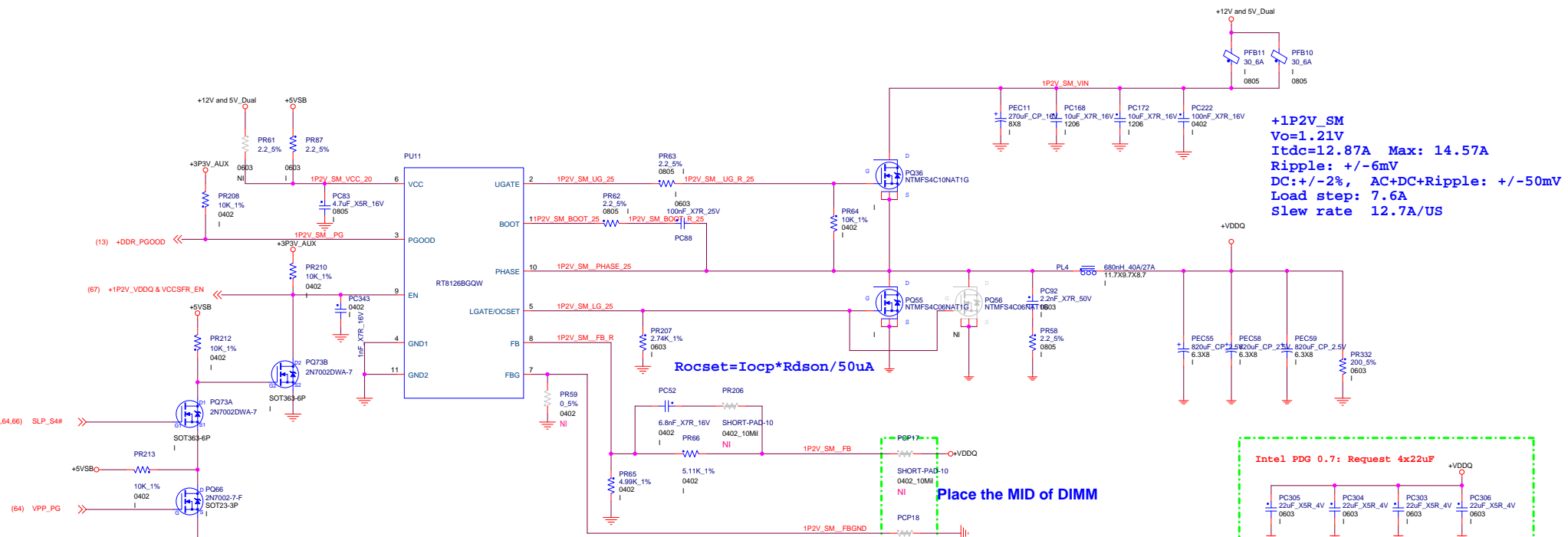


For Multi Power ONLY

+3V_DUAL



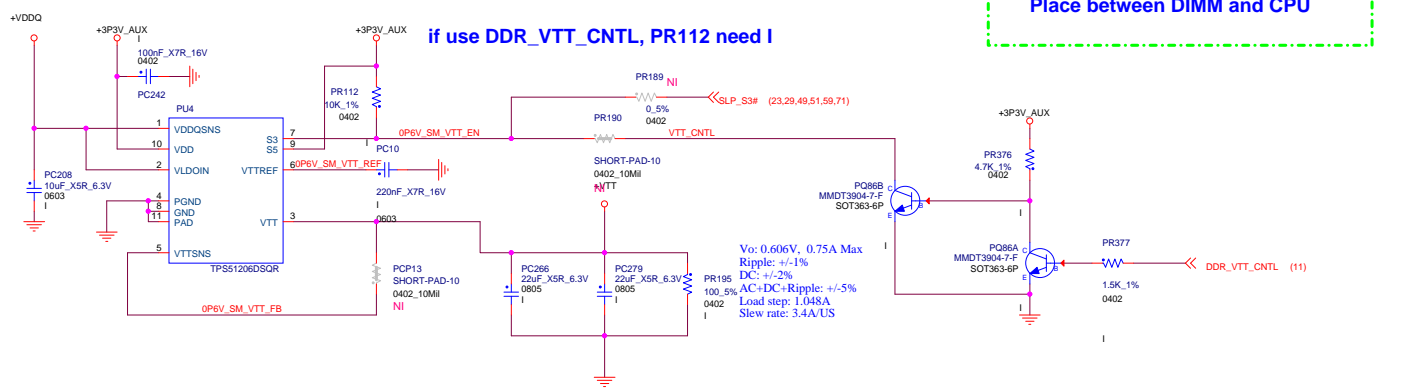
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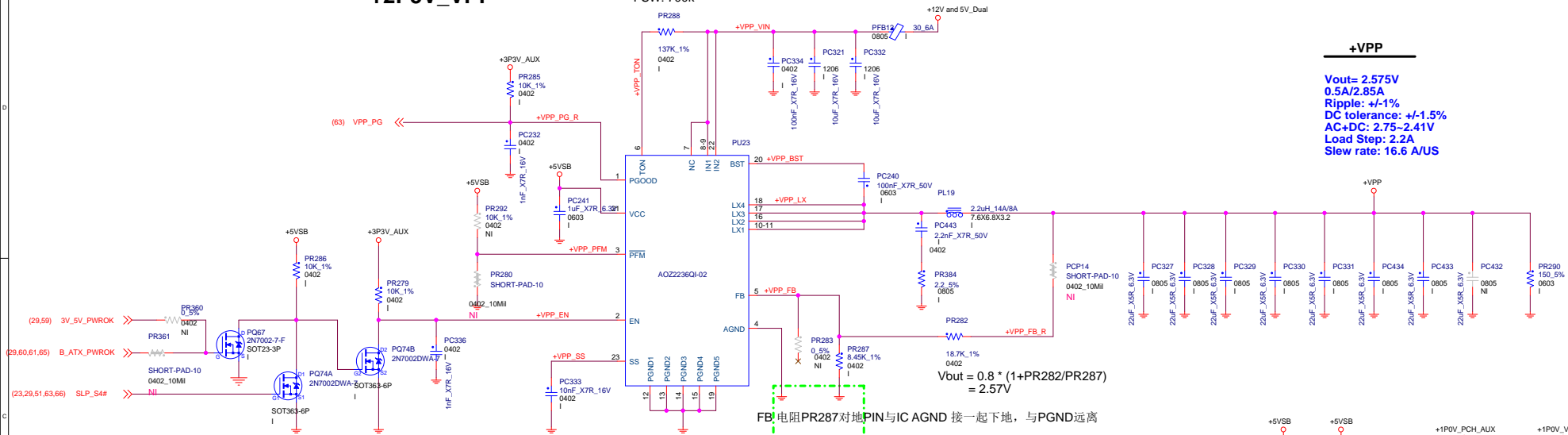
Table 1. Recommended Address Programming

Address	0x6A	0x68	0x66	0x64	0x62	0x60
R1 (kΩ)	open	3.9	3	2.3	1.3	10
R2 (kΩ)	10	1.3	2.3	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	40	60	75	100



+2P5V_VPP

Fsw_khz=38000*Vout/Rton_kohm
FSW: 700k

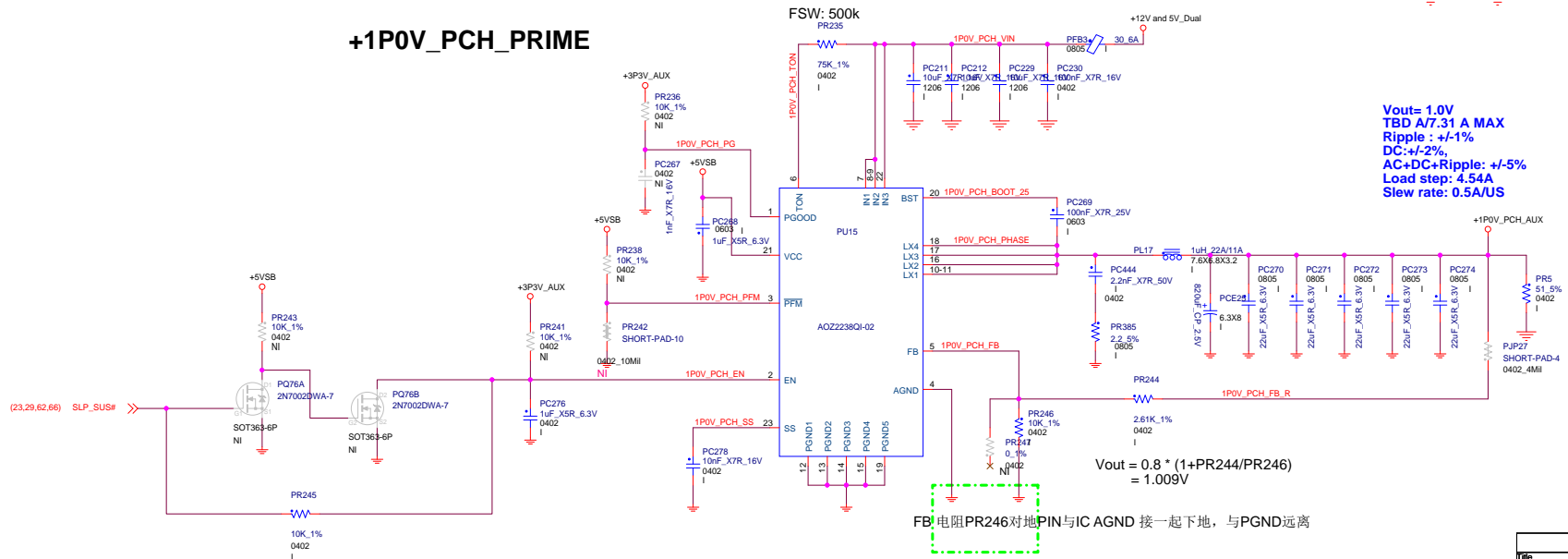


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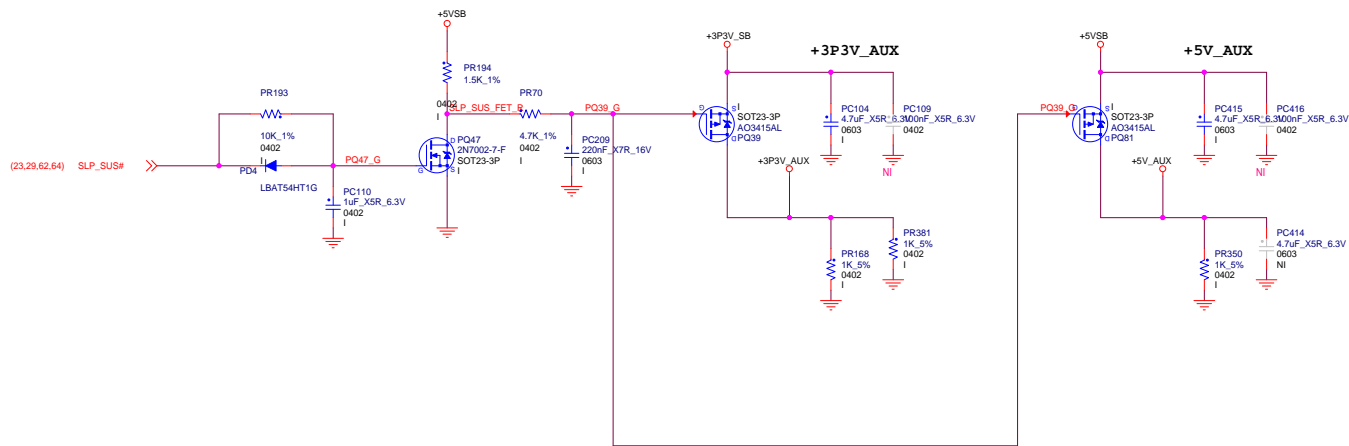
+1P0V_PCH_PRIME

Fsw_khz=38000*Vout/Rton_kohm

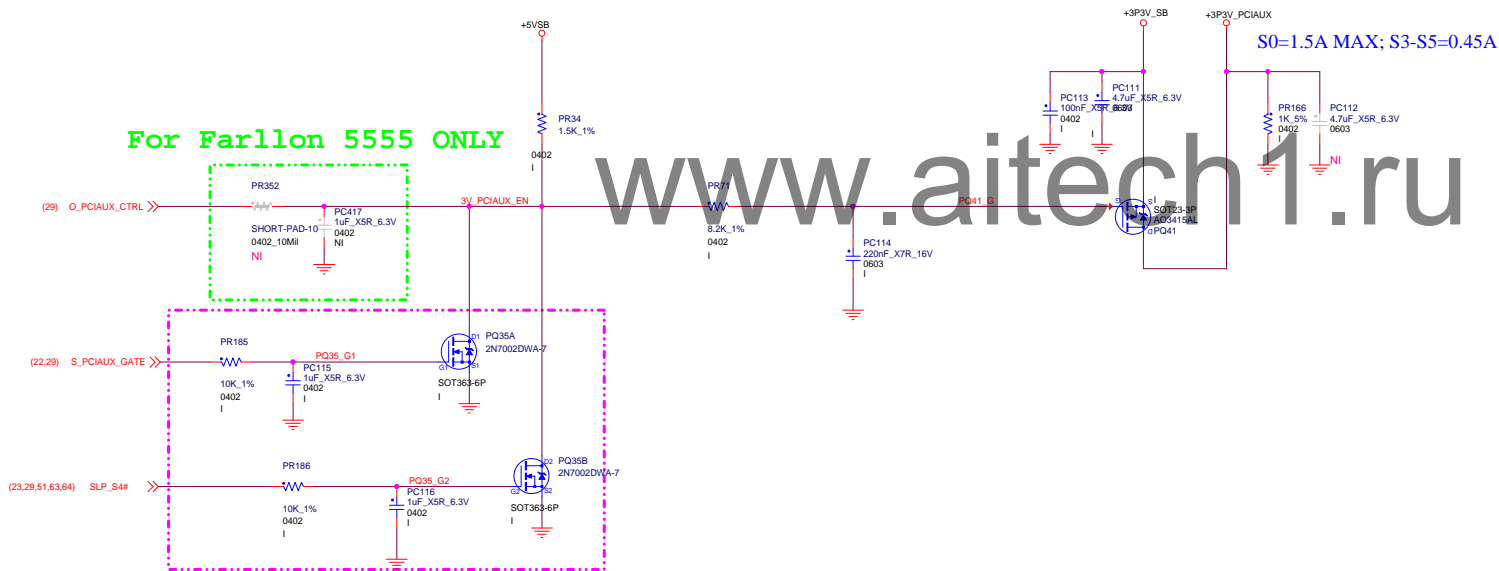
FSW: 500k

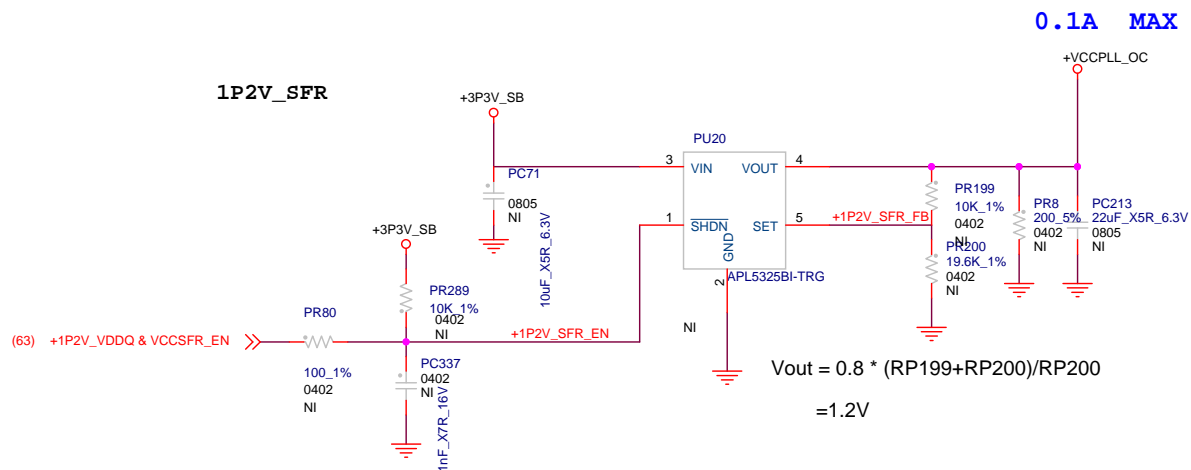


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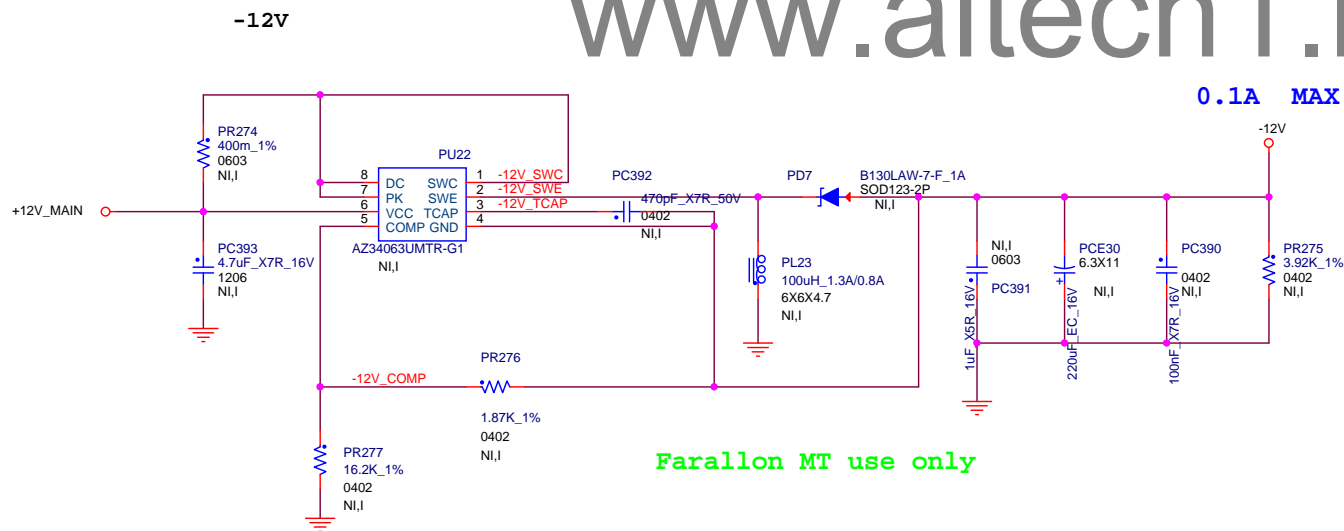


+3V_PCIAUX(FOR PCI/PCIE SLOT)

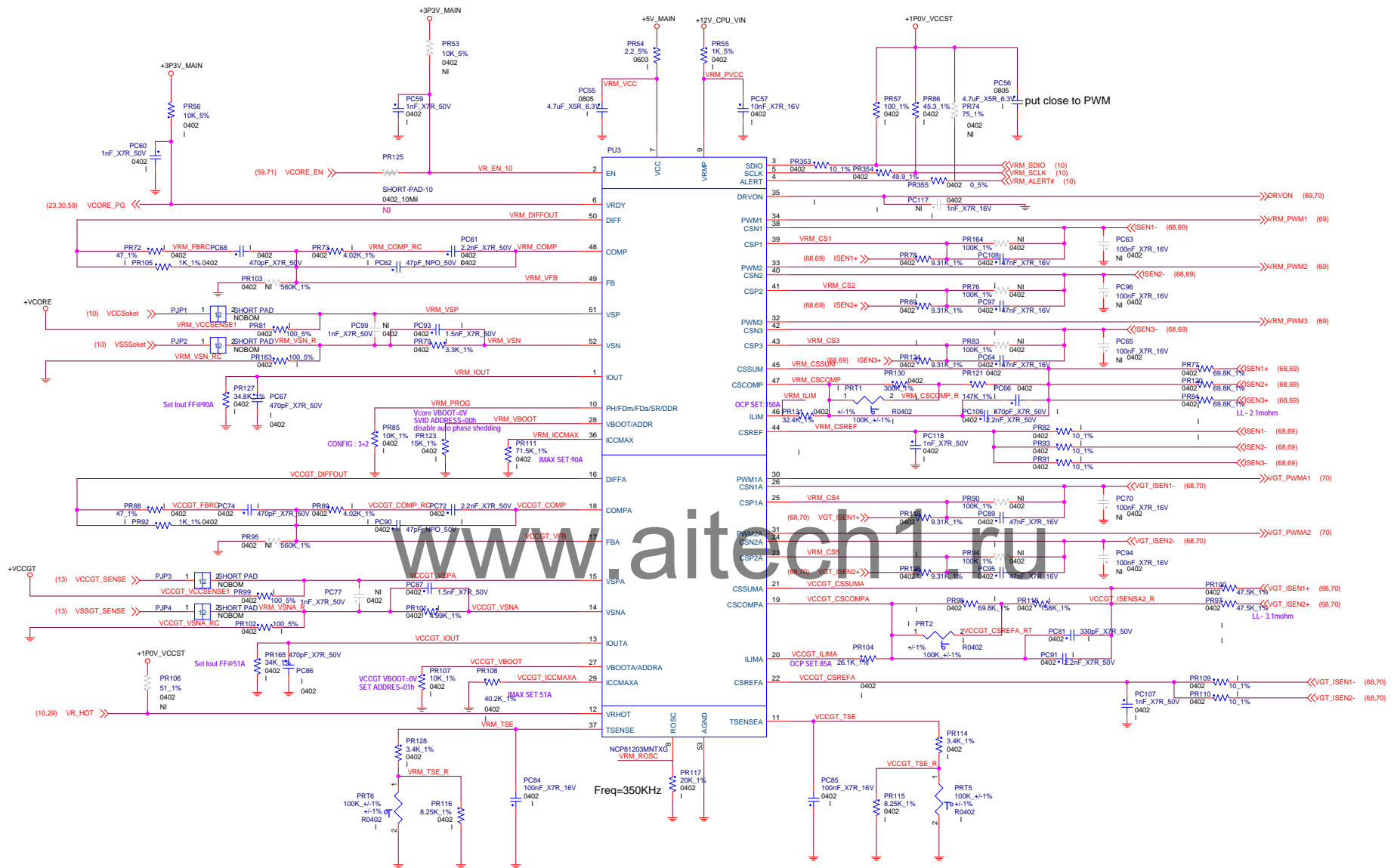




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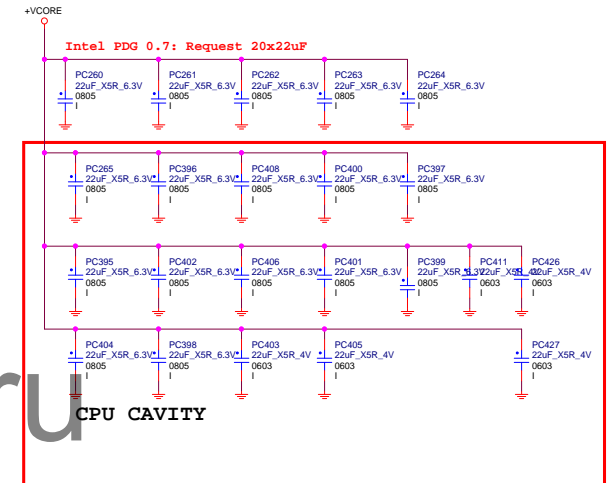
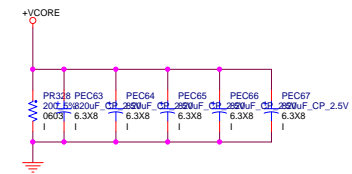
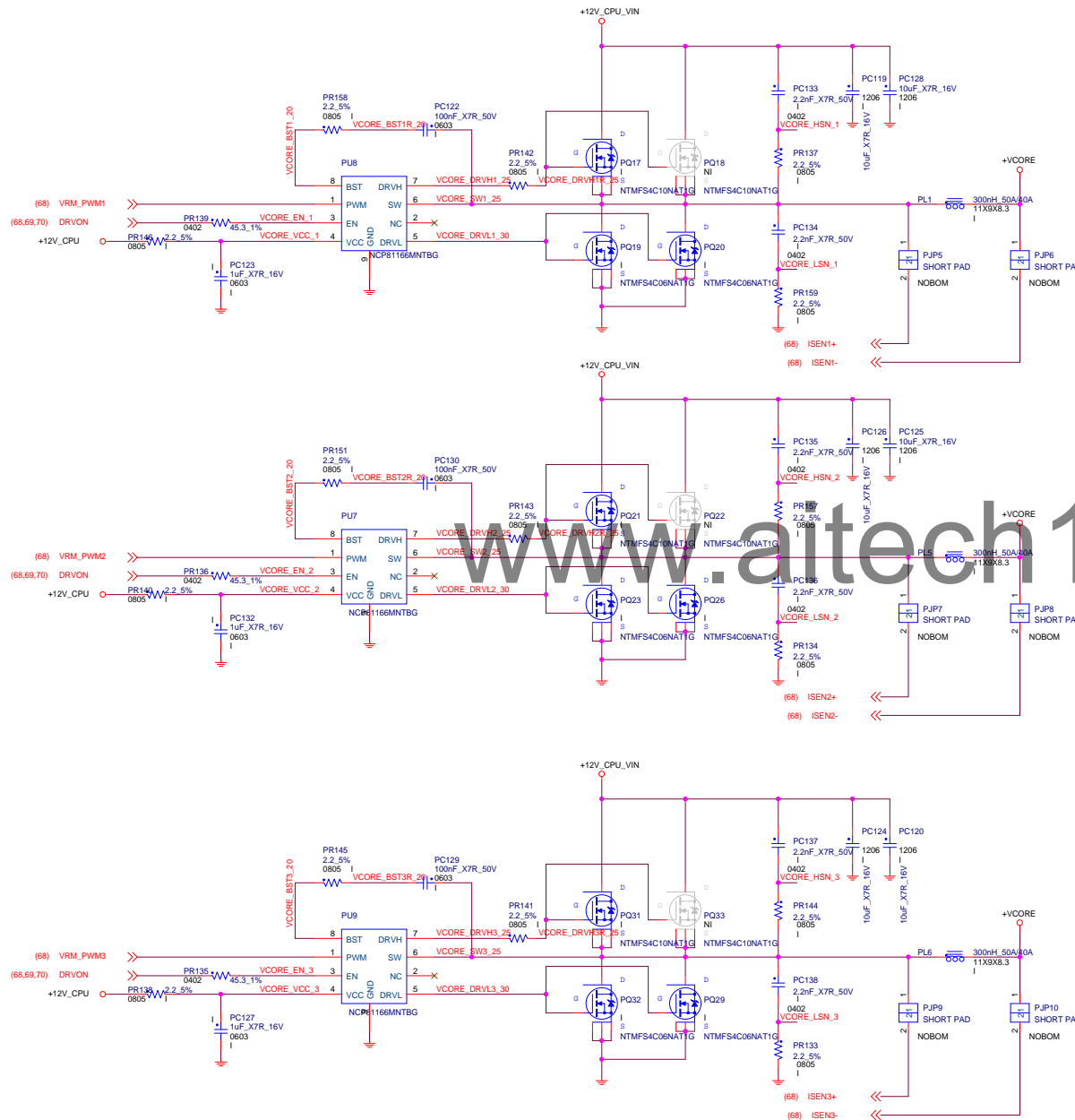
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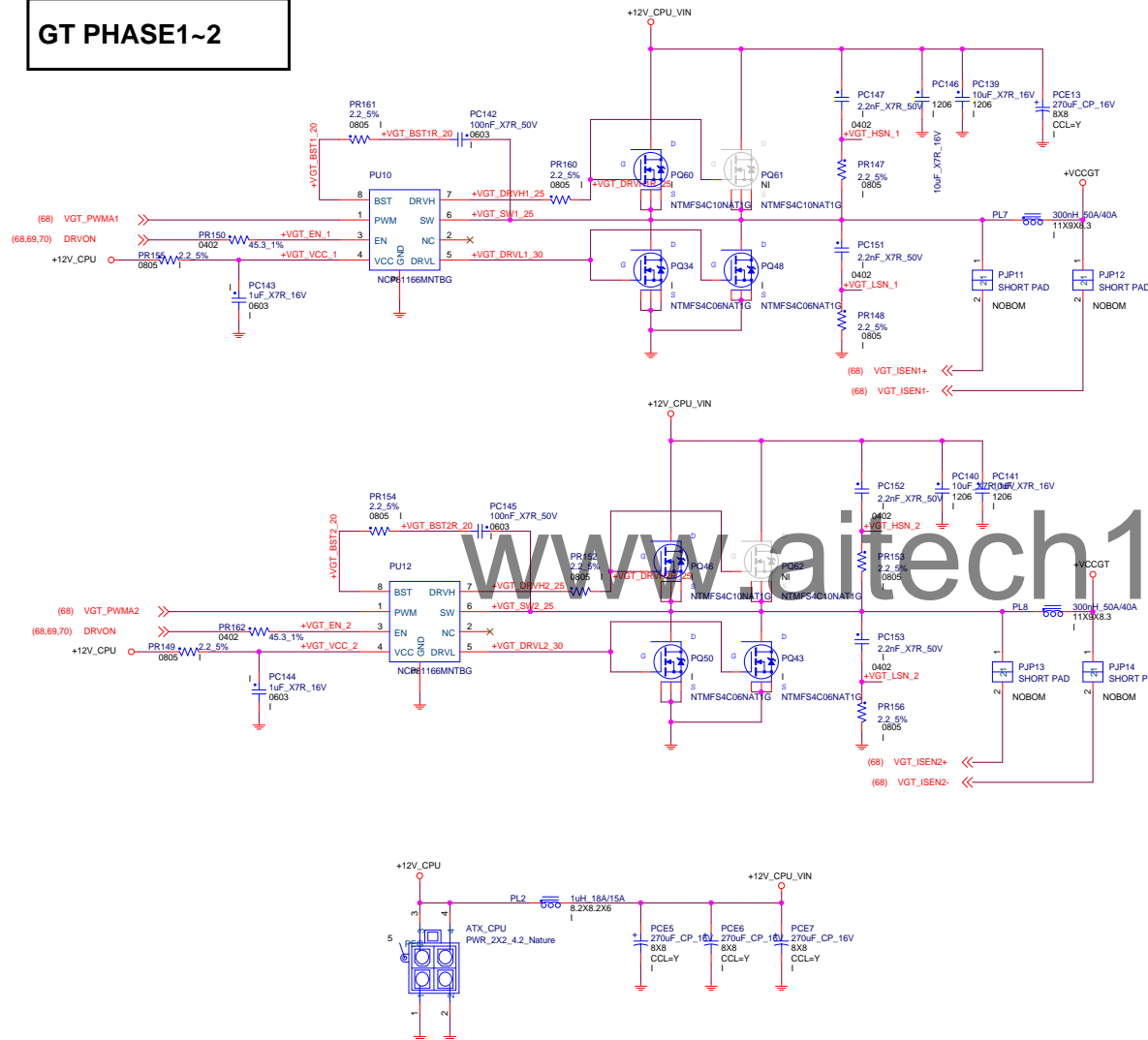
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VCORE PHASE1~3

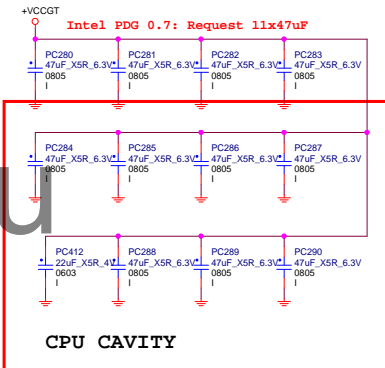
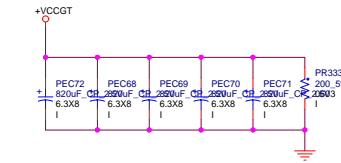
67A TDC / 90A MAX



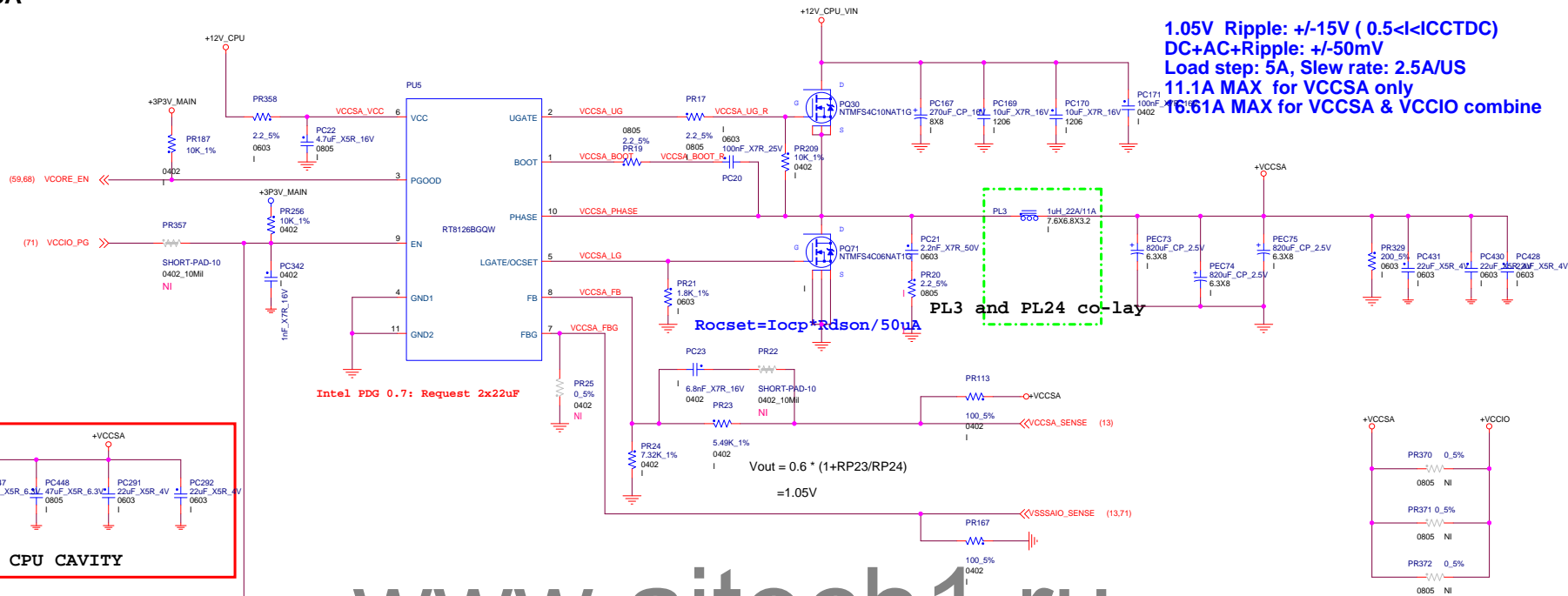
GT PHASE1~2



35A TDC / 51A MAX

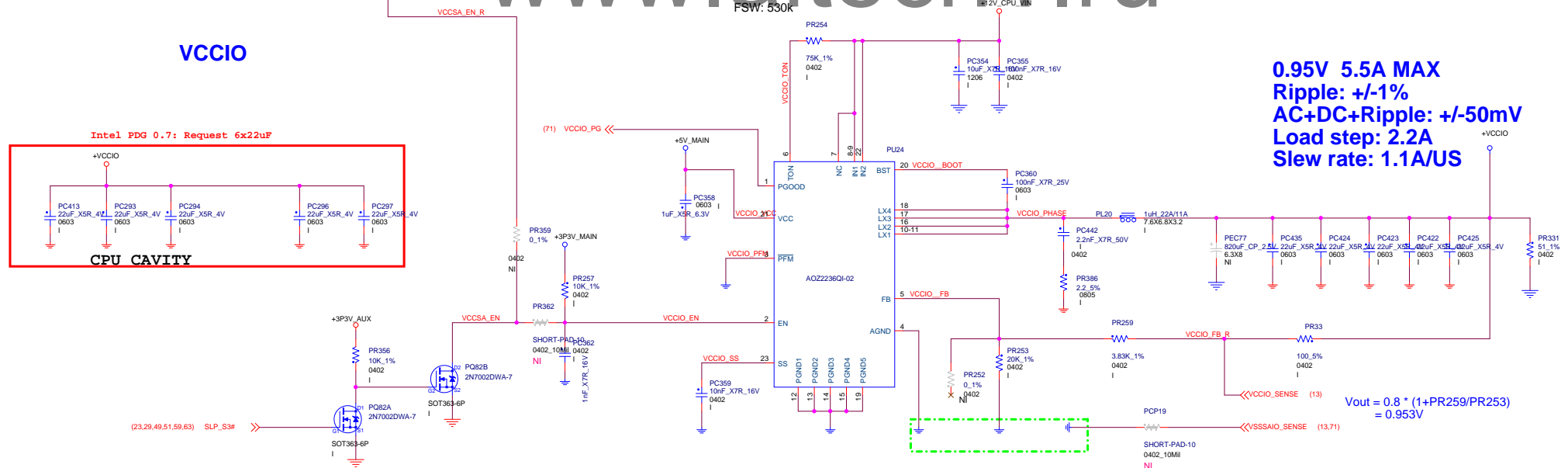


VCCSA



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VCCIO



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